



True-Color ChronDAC™ with 16-bit Interface

Features

- 16-bit pixel bus interface
- On-chip clock doubler
- Three high speed 8-bit 110/135 MHz DACs
- Three high speed 256 x 6-bit color palette RAMs
- Compatible with ATT20C498 display modes
- MIX-COLOR®: true on-the-fly mode switching
- 16.7M, 64K, 32K, and 256 color modes
- Supports 128/256 pseudo color, HICOLOR™2, 64K bypass, 16.7M bypass, XGA™ mode 2, and MIX-COLOR®
- Internal/external voltage reference or external current reference
- Drives singly or doubly terminated 75 Ω loads
- ID register for software identification
- Power down features for “Green PC” applications
- Anti-sparkle circuitry
- Dual-programmable 135 MHz PLL clocks
- On-chip loop filters for PLL clocks
- Pin compatible to SGS-Thomson STG1703
- Low power CMOS technology in 68-pin PLCC
- 5V supply

Description

The CH8398A *ChronDAC™* integrates two programmable PLLs, a triple 256 x 6-bit palette RAM, and a triple 8-bit 110/135 MHz video DAC. The video clock PLL provides 16 programmable frequencies, and the memory clock PLL provides 8 programmable frequencies.

The CH8398A pixel bus is 16 bits, twice the bandwidth of an 8-bit LUTDAC. The on-chip clock doubler allows CH8398A to support more colors with higher resolution while maintaining a lower pixel transfer rate.

Upon power up, the video clock is preset to 28.322 MHz and memory clock is preset to 40 MHz. After power up, video BIOS or driver software can initialize the PLL RAM entries to the desired values.

MIX-COLOR® mode provides the simultaneous display of maximum spatial resolution and color depth within a single bitmapped frame, efficiently utilizing memory. True on-the-fly mode switching occurs on a pixel-by-pixel basis, allowing 128/256 pseudo-color mode to be mixed with 64K color 5-6-5 or 32K color 5-5-5 bypass. Mixed mode switching can be controlled by hardware or software, easing design implementation.

CH8398A is fully compatible with VGA, VESA, Super-VGA, XGA™, TARGA™, 8514, and other non-standard frequencies, while providing many other enhanced features.

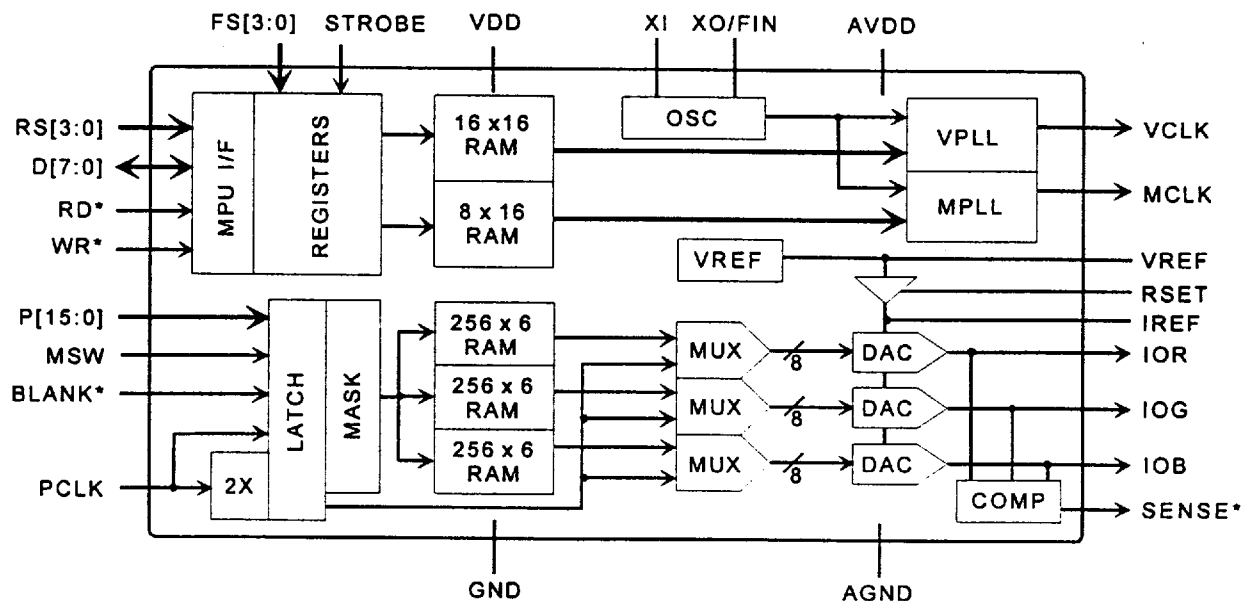


Figure 1: Block Diagram

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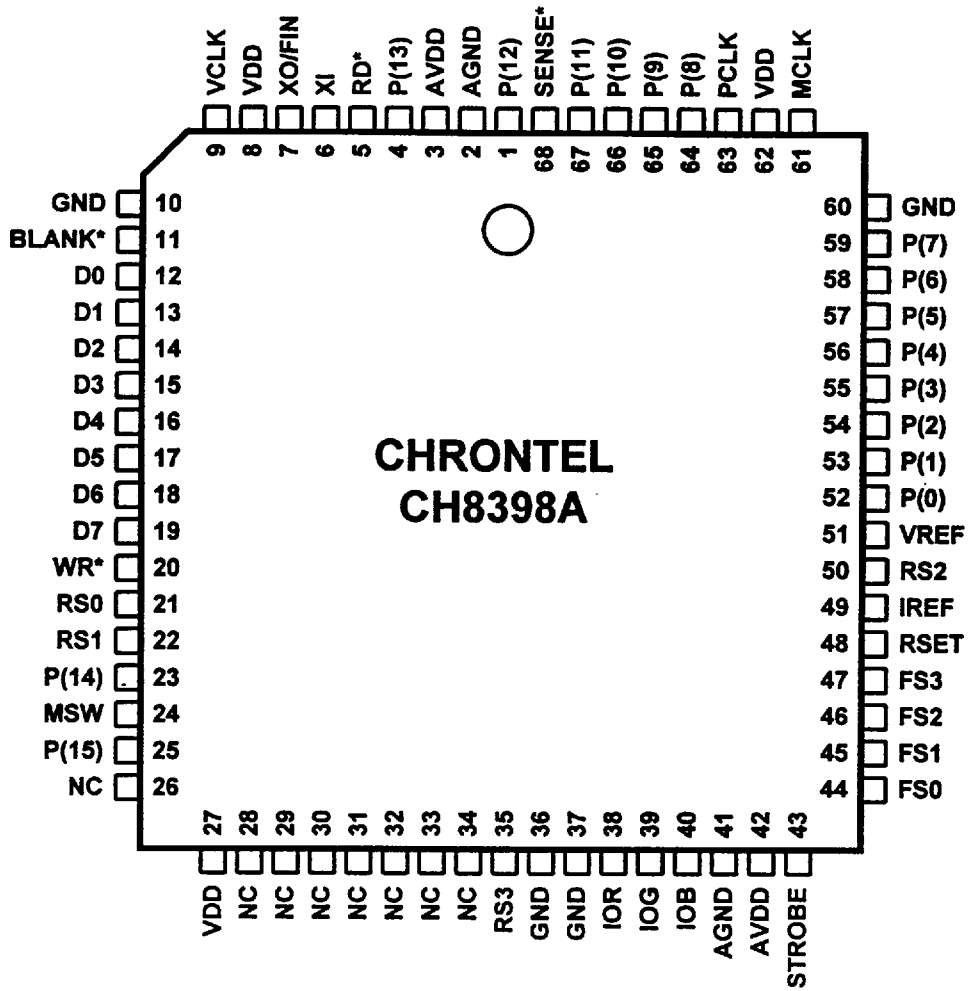


Figure 2: CH8398A

Table 1 • Pin Description

| Pin # | Symbol | Type | Name / Description |
|--------------------------------------|---|------|---|
| 1, 4, 23, 25, 52 – 59, 64 – 67 | P12, P13, P14, P15, P0 – P7, P8 – P11 | I | Pixel. TTL compatible. Pixel data is latched on the rising edge of PCLK. Pseudo-color mode: pixel data is used as an address map to color palette RAM. Bypass color mode: pixel data represents actual color and directly drives DACs. |
| 2, 41 | AGND | P | Analog Ground. AGND pins must be connected to system ground. |
| 3, 42 | AVDD | P | Analog Power. AVDD pins must be connected to +5V. |
| 5 | RD* | I | Read (Active Low). TTL compatible. RS[3:0] data is latched and transferred from selected register to data bus on falling edge of RD*. |
| 6 | XI | I | Crystal Oscillator. 14.318 MHz crystal or connect to GND if XO / FIN is connected to an external reference clock. |
| 7 | XO / FIN | I/O | Crystal Oscillator / External Frequency. 14.318 MHz crystal or external reference clock input. |
| 8, 27, 62 | VDD | P | Digital Power. VDD pins must be connected to +5V. |
| 9 | VCLK | O | Video Clock. TTL compatible. 28.322 MHz upon power up. |
| 10, 36, 37, 60 | GND | P | Digital Ground. GND pins must be connected to system ground. |
| 11 | BLANK* | I | Blank (Active Low). TTL compatible. BLANK* is latched on the rising edge of PCLK. When asserted, the analog outputs are turned off and the pixel inputs are ignored. |
| 12 – 19 | D0 – D7 | I/O | Data Bus. TTL compatible. Bi-directional data bus. |
| 20 | WR* | I | Write (Active Low). TTL compatible. RS[3:0] data is latched on falling edge of WR*. D[7:0] data is latched on rising edge of WR*. |
| 21, 22, 35, 50 | RS0, RS1, RS3, RS2 | I | Register Select. TTL compatible. RS[3:0] data is latched on falling edge of RD* or WR*. RS[3:0] inputs determine which internal register to access. RS3 pin is internally pulled up to VDD. |
| 24 | MSW | I | Mode Switch. TTL compatible with internal pull-down resistor. MSW is latched on the rising edge of PCLK. MSW input enables on-the-fly mode switching between primary and secondary modes. |
| 26, 28 – 34 | NC | — | No Connect. Unconnected pins. |
| 38, 39, 40 | IOR, IOG, IOB | O | Color Signals Output. Red, green, and blue DAC outputs, high impedance current sources capable of driving singly or doubly terminated 75 Ω load directly. |
| 43 | STROBE | I | Strobe. TTL compatible with internal pull-up resistor. FS[3:0] inputs are latched on the falling edge of STROBE. The STROBE control pin should be held at VDD or left open for direct pass-through of FS[3:0]. For further details, please refer to Figure 22 on page 45. |
| 44 – 47 | FS0 – FS3 | I | External Video Clock Select. TTL compatible with internal pull-down resistor. FS[3:0] inputs are bit-wise "OR"ed with internal register CSR [3:0]. |
| 48 | RSET | A | Reference Resistor. This pin should be connected through an external 147 Ω ± 1% resistor to GND. DAC output current levels are controlled by this resistor. See Note 2 below. |
| 49 | IREF | A | Current Reference. External current reference input. |
| 51 | VREF | A | Voltage Reference. If using an external voltage source, supply this input with a 1.23V reference. |
| 63 | PCLK | I | Pixel Clock. TTL compatible. Pixel data is latched on the rising edge of PCLK. |
| 61 | MCLK | O | Memory Clock. TTL compatible. 40 MHz upon power up. |
| 68 | SENSE* | O | Sense (Active Low). TTL compatible. Monitor detect signal. SENSE* is logical 0 if one or more of the IOR, IOG, and IOB outputs has exceeded the internal voltage reference level of 340 mV. |

Note 1:

- I Input signal
- O Output signal
- I/O Bi-directional signal
- P Power pins
- A Analog signal

Note 2:

$$I_{FS} = \frac{V_{REF}}{R_{SET}} \times 2.1$$

where

- IFS is full-scale output current
- VREF is the voltage reference with value 1.23V
- RSET is the resistor connected between the RSET pin and ground, typical value is 147 Ω ± 1%

Comparison of CH8398 and CH8398A

The following changes have been made in the CH8398A:

| FEATURES | CH8398 | CH8398A |
|--|------------|-------------|
| RS2 required to access PLL RAM (page 33) | Yes | No |
| PLL parameter N values restricted (page 39) | Yes | No |
| VPLL RAM Locations 0 and 1 (page 36) | Hard-wired | Initialized |
| Reserved bits in Auxiliary Register (AUXR) (page 32) | 4 | 1 |
| Changes in AUXR definitions (page 32) | — | Yes |

Note: Changes have been highlighted on pages indicated

Display Modes

Chronitel CH8398A offers two basic color modes: pseudo and bypass.

Pseudo-color mode: Pixel address (8-bit), after being logically "AND"ed with the pixel Read Mask Register (RMR), is used to address all red, green, and blue palette RAM.

Bypass color mode: Pixel data is used to drive inputs of the DACs directly, bypassing the palette RAM and the RMR.

CH8398A provides 14 different display modes, each consisting of a primary and secondary mode. The pixel-by-pixel mode switching between primary and secondary modes is accomplished on-the-fly, and can be achieved through either hardware or software control.

Table 2 • Summary of Display Modes

| Mode | CR[7:4] | MSW = 0, PRIMARY MODE | | Primary Mode Description | Colors |
|------|---------|-------------------------|--|--|--------|
| 0* | 0000 | 8B1P1C | 8 bpp, 1 pixel address, 1 PCLK cycle | 8-bit pseudo | 256 |
| 1* | 0001 | 15B1P1C | 15 bpp, 1 pixel data, 1 PCLK cycle | 15-bit 5-5-5 bypass | 32K |
| 2*† | 0010 | 8B2P1C | 8 bpp, 2 pixel addresses, 1 PCLK cycle | 8-bit pseudo | 256 |
| 3* | 0011 | 16B1P1C | 16 bpp, 1 pixel data, 1 PCLK cycle | 16-bit 5-6-5 bypass | 64K |
| 4* | 0100 | 8B1P2C (4 + 4) | 8 bpp, 1 pixel address, 2 PCLK cycles | 8-bit pseudo (4 + 4 pixel data transfer) | 256 |
| 5* | 0101 | 24B1P2C | 24 bpp, 1 pixel data, 2 PCLK cycles | 24-bit 8-8-8 bypass | 16.7M |
| 6* | 0110 | 16B1P2C | 16 bpp, 1 pixel data, 2 PCLK cycles | 16-bit 5-6-5 bypass | 64K |
| 7* | 0111 | 24B1P3C | 24 bpp, 1 pixel data, 3 PCLK cycles | 24-bit 8-8-8 bypass | 16.7M |
| 8* | 1000 | 8B1P2C (4 + 4) | 8 bpp, 1 pixel address, 2 PCLK cycles | 8-bit pseudo (4 + 4 pixel data transfer) | 256 |
| 9* | 1001 | 8B1P2C (8 + 0) | 8 bpp, 1 pixel address, 2 PCLK cycles | 8-bit pseudo (8 + 0 pixel data transfer) | 256 |
| A† | 1010 | 8B2P1C | 8 bpp, 2 pixel addresses, 1 PCLK cycle | MIX-COLOR®, 8-bit pseudo | 256 |
| B† | 1011 | 24B2P3C | 24 bpp, 2 pixel data, 3 PCLK cycles | 24-bit 8-8-8 bypass | 16.7M |
| C | 1100 | 15B1P2C | 15 bpp, 1 pixel data, 2 PCLK cycles | 15-bit 5-5-5 bypass | 32K |
| D† | 1101 | 8B2P1C | 8 bpp, 2 pixel addresses, 1 PCLK cycle | MIX-COLOR®, 8-bit pseudo | 256 |
| Mode | CR[7:4] | MSW = 1, SECONDARY MODE | | Secondary Mode Description | Colors |
| 0* | 0000 | 16B1P1C | 16 bpp, 1 pixel data, 1 PCLK cycle | 16-bit 5-6-5 bypass | 64K |
| 1* | 0001 | 8B1P1C | 8 bpp, 1 pixel address, 1 PCLK cycle | 8-bit pseudo | 256 |
| 2*† | 0010 | 8B2P1C | 8 bpp, 2 pixel addresses, 1 PCLK cycle | 8-bit pseudo | 256 |
| 3* | 0011 | 8B1P1C | 8 bpp, 1 pixel address, 1 PCLK cycle | 8-bit pseudo | 256 |
| 4* | 0100 | 24B1P2C | 24 bpp, 1 pixel data, 2 PCLK cycles | 24-bit 8-8-8 bypass | 16.7M |
| 5* | 0101 | 16B1P2C | 16 bpp, 1 pixel data, 2 PCLK cycles | 16-bit 5-6-5 bypass | 64K |
| 6* | 0110 | 24B1P2C | 24 bpp, 1 pixel data, 2 PCLK cycles | 24-bit 8-8-8 bypass | 16.7M |
| 7* | 0111 | 24B1P3C | 24 bpp, 1 pixel data, 3 PCLK cycles | 24-bit 8-8-8 bypass | 16.7M |
| 8* | 1000 | 16B1P2C | 16 bpp, 1 pixel data, 2 PCLK cycles | 16-bit 5-6-5 bypass | 64K |
| 9* | 1001 | 24B1P2C | 24 bpp, 1 pixel data, 2 PCLK cycles | 24-bit 8-8-8 bypass | 16.7M |
| A† | 1010 | 15B1P1C | 15 bpp, 1 pixel data, 1 PCLK cycle | MIX-COLOR®, 15-bit 5-5-5 bypass | 32K |
| B† | 1011 | 24B2P3C | 24 bpp, 2 pixel data, 3 PCLK cycles | 24-bit 8-8-8 bypass | 16.7M |
| C | 1100 | 8B1P2C (4 + 4) | 8 bpp, 1 pixel address, 2 PCLK cycles | 8-bit pseudo (4 + 4 pixel data transfer) | 256 |
| D† | 1101 | 16B1P1C | 16 bpp, 1 pixel data, 1 PCLK cycle | MIX-COLOR®, 16-bit 5-6-5 bypass | 64K |

Note: bpp = bits per pixel † = on-chip clock doubler enabled * = ATT20C498 compatible mode

Display Modes (continued)

See Table 2 on page 7 for detailed pixel data organization.

Mode 0

Primary Mode: **8B1P1C:** 8 bpp, 1 pixel address, 1 PCLK cycle, 256 colors

Pixel address for the red, green, and blue color palette is latched on the rising edge of PCLK. Palette RAM contains 256 colors of 256K possible colors (6 bits each for the IOR, IOG, and IOB outputs). Pseudo color pixel address (P[7:0]) is then bit-wise "AND"ed with the pixel RMR.

Following is the **8B1P1C** pixel address transfer format:

| P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| X | X | X | X | X | X | X | X | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

Note: **bpp** = bits per pixel
 P[i] = pixel input pin

X = unused bit
 P[7:0] = pseudo color pixel address

Secondary Mode: **16B1P1C:** 16 bpp (5-6-5), 1 pixel data, 1 PCLK cycle, 64K colors

Pixel data is latched on the rising edge of PCLK. Pixel data is organized as 5 bits of color information for red and blue, and 6 bits of color information for the green color palette. For further information, please refer to **Figure 6** on page 20.

Following is the **16B1P1C (5-6-5)** pixel data transfer format:

| P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| R7 | R6 | R5 | R4 | R3 | G7 | G6 | G5 | G4 | G3 | G2 | B7 | B6 | B5 | B4 | B3 |

Note: Lowest two or three bits of the DAC inputs are padded with zeros

bpp = bits per pixel
 R[7:3] = red pixel data

P[i] = pixel input pin
 G[7:2] = green pixel data

B[7:3] = blue pixel data

Display Modes (continued)

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Mode 1

Primary Mode: **15B1P1C:** 15 bpp (5-5-5), 1 pixel data, 1 PCLK cycle, 32K colors

Pixel data is latched on the rising edge of PCLK. Pixel data is organized as 5 bits of color information each for the red, green, and blue color palette. For further information, please refer to **Figure 5** on page 20.

Following is the **15B1P1C (5-5-5)** pixel data transfer format:

| P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| X | R7 | R6 | R5 | R4 | R3 | G7 | G6 | G5 | G4 | G3 | B7 | B6 | B5 | B4 | B3 |

Note: Lowest three bits of the DAC inputs are padded with zeros

bpp = bits per pixel

X = unused bit

P[i] = pixel input pin

R[7:3] = red pixel data

G[7:3] = green pixel data

B[7:3] = blue pixel data

Secondary Mode: **8B1P1C:** 8 bpp, 1 pixel address, 1 PCLK cycle, 256 colors

Pixel address for the red, green, and blue color palette is latched on the rising edge of PCLK. Palette RAM contains 256 colors of 256K possible colors (6 bits each for the IOR, IOG, and IOB outputs). Pseudo color pixel address (P[7:0]) is then bit-wise "AND"ed with the pixel RMR.

Following is the **8B1P1C** pixel address transfer format:

| P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| X | X | X | X | X | X | X | X | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

Note: **bpp** = bits per pixel

X = unused bit

P[i] = pixel input pin

P[7:0] = pseudo color pixel address

Display Modes (continued)

Mode 2

Primary /

Secondary Modes: **8B2P1C:** 8 bpp, 2 pixel addresses, 1 PCLK cycle, 256 colors

Pixel addresses for the red, green, and blue color palette are latched on the rising edge of PCLK. Palette RAM contains 256 colors of 256K possible colors (6 bits each for the IOR, IOG, and IOB outputs). Pseudo color pixel addresses (P[7:0]) are then bit-wise "AND"ed with the RMR.

Following is the **8B2P1C** pixel address transfer format:

| | | | | | | | | | | | | | | | |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

Note: Internal clock doubler enabled to produce twice the pixel resolution per PCLK period

bpp = bits per pixel

P[i] = pixel input pin

P[7:0] = pseudo color pixel address

Mode 3

Primary Mode:

16B1P1C: 16 bpp (5-6-5), 1 pixel data, 1 PCLK cycle, 64K colors

Pixel data is latched on the rising edge of PCLK. Pixel data is organized as 5 bits of color information for red and blue, and 6 bits of color information for the green color palette. For further information, please refer to **Figure 6** on page 20.

Following is the **16B1P1C (5-6-5)** pixel data transfer format:

| | | | | | | | | | | | | | | | |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
| R7 | R6 | R5 | R4 | R3 | G7 | G6 | G5 | G4 | G3 | G2 | B7 | B6 | B5 | B4 | B3 |

Note: Lowest two or three bits of the DAC inputs are padded with zeros

bpp = bits per pixel

P[i] = pixel input pin

B[7:3] = blue pixel data

R[7:3] = red pixel data

G[7:2] = green pixel data

Secondary Mode:

8B1P1C: 8 bpp, 1 pixel address, 1 PCLK cycle, 256 colors

Pixel address for the red, green, and blue color palette is latched on the rising edge of PCLK. Palette RAM contains 256 colors of 256K possible colors (6 bits each for the IOR, IOG, and IOB outputs). Pseudo color pixel address (P[7:0]) is then bit-wise "AND"ed with the pixel RMR.

Following is the **8B1P1C** pixel address transfer format:

| | | | | | | | | | | | | | | | |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
| X | X | X | X | X | X | X | X | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

Note: bpp = bits per pixel

X = unused bit

P[i] = pixel input pin

P[7:0] = pseudo color pixel address

Display Modes (continued)

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Mode 8

Primary Mode: **8B1P2C:** 8 bpp (4 + 4), 1 pixel address, 2 PCLK cycles, 256 colors

Pixel address for the red, green, and blue color palette is latched on every two consecutive rising edges of PCLK. Palette RAM contains 256 colors of 256K possible colors (6 bits each for the IOR, IOG, and IOB outputs). Pseudo color pixel address (P[7:0]) is then bit-wise "AND"ed with the RMR.

Following is the **8B1P2C (4 + 4)** pixel address transfer format:

| | P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
|-----|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| 1st | X | X | X | X | X | X | X | X | X | X | X | X | P3 | P2 | P1 | P0 |
| 2nd | X | X | X | X | X | X | X | X | X | X | X | X | P7 | P6 | P5 | P4 |

Note: bpp = bits per pixel

X = unused bit

P[i] = pixel input pin

Secondary Mode: **16B1P2C:** 16 bpp (5-6-5), 1 pixel data, 2 PCLK cycles, 64K colors

Pixel data is latched on every two consecutive rising edges of PCLK. Pixel data is organized as 5 bits of color information for red and blue, and 6 bits of color information for the green color palette. For further information, please refer to **Figure 6** on page 20.

Following is the **16B1P2C (5-6-5)** pixel data transfer format:

| | P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
|-----|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| 1st | X | X | X | X | X | X | X | X | G4 | G3 | G2 | B7 | B6 | B5 | B4 | B3 |
| 2nd | X | X | X | X | X | X | X | X | R7 | R6 | R5 | R4 | R3 | G7 | G6 | G5 |

Note: Lowest two or three bits of the DAC inputs are padded with zeros

 bpp = bits per pixel

X = unused bit

P[i] = pixel input pin

R[7:3] = red pixel data

G[7:2] = green pixel data

B[7:3] = blue pixel data

1st = first pixel data latched in

2nd = second pixel data latched

Display Modes (continued)

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Mode A

Primary Mode: **8B2P1C:** 8 bpp, 2 pixel addresses, 1 PCLK cycle, 256 colors

Pixel addresses for the red, green, and blue color palette are latched on the rising edge of PCLK. Palette RAM contains 256 colors of 256K possible colors (6 bits each for the IOR, IOG, and IOB outputs). Pseudo color pixel addresses (P[7:0]) are then bit-wise "AND"ed with the RMR.

Following is the **8B2P1C** pixel address transfer format:

| | | | | | | | | | | | | | | | |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

Note: Internal clock doubler enabled to produce twice the pixel resolution per PCLK period
 bpp = bits per pixel P[i] = pixel input pin P[7:0] = pseudo color pixel address

Secondary Mode: **15B1P1C:** 15 bpp (5-5-5), 1 pixel data, 1 PCLK cycle, 32K colors

Pixel data is latched on the rising edge of PCLK. Pixel data is organized as 5 bits of color information each for the red, green, and blue color palette. For further information, please refer to **Figure 5** on page 20.

Following is the **15B1P1C (5-5-5)** pixel data transfer format:

| | | | | | | | | | | | | | | | |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
| X | R7 | R6 | R5 | R4 | R3 | G7 | G6 | G5 | G4 | G3 | B7 | B6 | B5 | B4 | B3 |

Note: Lowest three bits of the DAC inputs are padded with zeros
 bpp = bits per pixel X = unused bit P[i] = pixel input pin
 R[7:3] = red pixel data G[7:3] = green pixel data B[7:3] = blue pixel data

Mode B

Primary /

Secondary Modes: **24B2P3C:** 24 bpp (8-8-8), 2 pixel data, 3 PCLK cycles, 16.7M colors

Pixel data is latched on every three consecutive rising edges of PCLK. Pixel data is organized as 8 bits of color information each for the red, green, and blue color palette.

Following is the **24B2P3C (8-8-8)** pixel data transfer format:

| | | | | | | | | | | | | | | | | |
|-----|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| | P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
| 1st | G7 | G6 | G5 | G4 | G3 | G2 | G1 | G0 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 2nd | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 |
| 3rd | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | G7 | G6 | G5 | G4 | G3 | G2 | G1 | G0 |

Note: Internal clock doubler enabled to produce twice the pixel resolution per PCLK period
 bpp = bits per pixel P[i] = pixel input pin
 R[7:0] = red pixel data G[7:0] = green pixel data B[7:0] = blue pixel data
 1st = first pixel data latched in 2nd = second pixel data latched 3rd = third pixel data latched

Display Modes (continued)

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Mode C

Primary Mode:

15B1P2C: 15 bpp (5-5-5), 1 pixel data, 2 PCLK cycles, 32K colors

Pixel data is latched on every two consecutive rising edges of PCLK. Pixel data is organized as 5 bits of color information each for the red, green, and blue color palette. For further information, please refer to **Figure 5** on page 20.

Following is the **15B1P2C (5-5-5)** pixel data transfer format:

| | P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
|-----|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| 1st | X | X | X | X | X | X | X | X | G5 | G4 | G3 | B7 | B6 | B5 | B4 | B3 |
| 2nd | X | X | X | X | X | X | X | X | X | R7 | R6 | R5 | R4 | R3 | G7 | G6 |

Note: Lowest three bits of DAC inputs are padded with zeros

bpp = bits per pixel

X = unused bit

P[i] = pixel input pin

R[7:3] = red pixel data

G[7:3] = green pixel data

B[7:3] = blue pixel data

1st = first pixel data latched in

2nd = second pixel data latched

Secondary Mode:

8B1P2C: 8 bpp (4 + 4), 1 pixel address, 2 PCLK cycles, 256 colors

Pixel address for the red, green, and blue color palette is latched on every two consecutive rising edges of PCLK. Palette RAM contains 256 colors of 256K possible colors (6 bits each for the IOR, IOG, and IOB outputs). Pseudo color pixel address (P[7:0]) is then bit-wise "AND"ed with the RMR.

Following is the **8B1P2C (4 + 4)** pixel address transfer format:

| | P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
|-----|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| 1st | X | X | X | X | X | X | X | X | X | X | X | X | P3 | P2 | P1 | P0 |
| 2nd | X | X | X | X | X | X | X | X | X | X | X | X | P7 | P6 | P5 | P4 |

Note: bpp = bits per pixel

X = unused bit

P[i] = pixel input pin

Display Modes (continued)

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Mode D

Primary Mode: **8B2P1C:** 8 bpp, 2 pixel addresses, 1 PCLK cycle, 256 colors

Pixel addresses for the red, green, and blue color palette are latched on the rising edge of PCLK. Palette RAM contains 256 colors of 256K possible colors (6 bits each for the IOR, IOG, and IOB outputs). Pseudo color pixel addresses (P[7:0]) are then bit-wise "AND"ed with the RMR.

Following is the **8B2P1C** pixel address transfer format:

| | | | | | | | | | | | | | | | |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

Note: Internal clock doubler enabled to produce twice the pixel resolution per PCLK period
 bpp = bits per pixel P[7:0] = pseudo color pixel address P[i] = pixel input pin

Secondary Mode: **16B1P1C:** 16 bpp (5-6-5), 1 pixel data, 1 PCLK cycle, 64K colors

Pixel data is latched on the rising edge of PCLK. Pixel data is organized as 5 bits of color information for red and blue, and 6 bits of color information for the green color palette. For further information, please refer to **Figure 6** on page 20.

Following is the **16B1P1C (5-6-5)** pixel data transfer format:

| | | | | | | | | | | | | | | | |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
| R7 | R6 | R5 | R4 | R3 | G7 | G6 | G5 | G4 | G3 | G2 | B7 | B6 | B5 | B4 | B3 |

Note: Lowest two or three bits of DAC inputs are padded with zeros
 bpp = bits per pixel P[i] = pixel input pin
 R[7:3] = red pixel data G[7:2] = green pixel data B[7:3] = blue pixel data

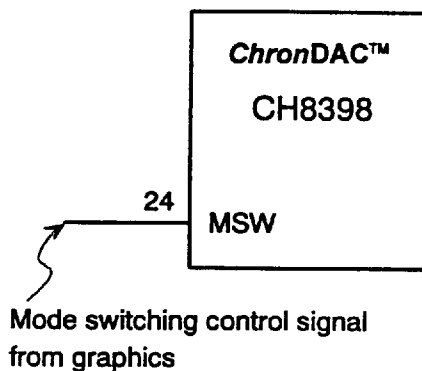
Hardware and Software Mode Switching

Hardware mode switching:

The external mode control pin (MSW) is used to switch between primary and secondary modes and requires bit 2 (MSDIS) = 0 (default value) in the Control Register (CR).

Primary mode: MSW = 0

Secondary mode: MSW = 1



Hardware mode switching

The external MSW signal (pin 24) handles the hardware mode switching for CH8398A.

The mode switching control signal from the graphics controller drives the MSW input on CH8398A.

Figure 3: Hardware Mode Switching

Software (embedded) mode switching: The mode control signal is used to switch between primary and secondary modes and is *embedded* in the pixel data.

Embedded switching can be applied to modes 1, 8, A, and C.

Mode A

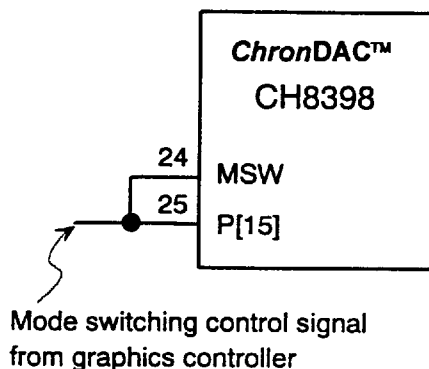
Primary mode: P[7] and P[15] = 0

Secondary mode: P[15] = 1

Modes 1, 8, and C

Primary mode: P[15] = 0

Secondary mode: P[15] = 1



Software mode switching

CH8398A handles software or embedded mode switching by connecting MSW and P[15] pins.

The mode switching control signal from the graphics controller drives MSW and P[15] inputs on CH8398A.

Note: Design flexibility utilizing either hardware or software (embedded) mode switching may be achieved by connecting pins through a 0 Ω resistor

Figure 4: Software Mode Switching

Note: Hardware mode switching method applies to all display modes
Software mode switching method is limited to certain display modes

Bypass Mode Diagrams

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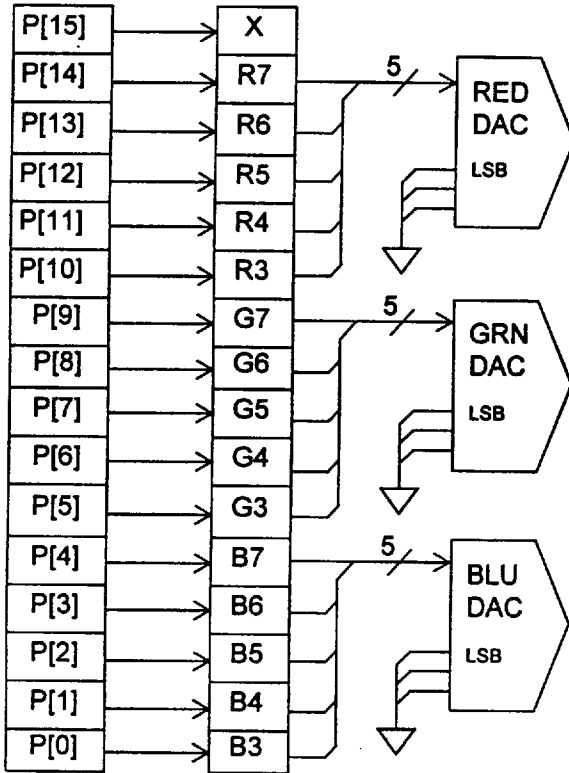


Figure 5: 15-bit bypass mode
(used in Modes 1, A, C)

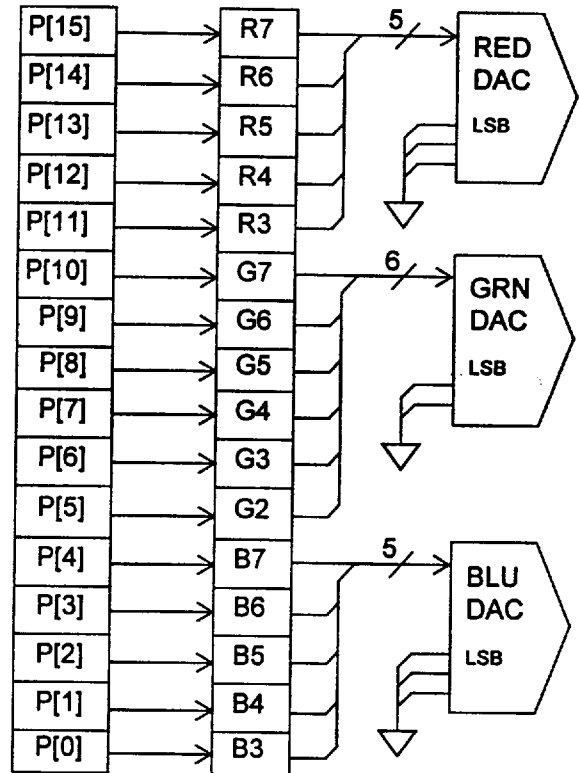


Figure 6: 16-bit bypass mode
(used in Modes 0, 3, 5, 6, 8, D)

Note: Lowest two or three bits of DAC inputs are padded with zeros
 P[i] = pixel input pin R[7:3] = red pixel data
 G[7:2] = green pixel data B[7:3] = blue pixel data

Table 3 • Pixel Data Organization

| Mode | MSW = 0 | | Organization of Pixel Inputs | | MSW = 1 | Organization of Pixel Inputs | |
|------|-------------------|---|---|-------------------|---|---|--------|
| | Prime | P[15:8] | P[7:0] | Second | | P[15:8] | P[7:0] |
| 0* | 8B1P1C | X X X X X X X X | P7 P6 P5 P4 P3 P2 P1 P0 | 16B1P1C | R7 R6 R5 R4 R3 G7 G6 G5 | G4 G3 G2 B7 B6 B5 B4 B3 | |
| 1* | 15B1P1C | X R7 R6 R5 R4 R3 G7 G6 | G5 G4 G3 B7 B6 B5 B4 B3 | 8B1P1C | X X X X X X X X | P7 P6 P5 P4 P3 P2 P1 P0 | |
| 2† | 8B2P1C | P7 P6 P5 P4 P3 P2 P1 P0 | P7 P6 P5 P4 P3 P2 P1 P0 | 8B2P1C | P7 P6 P5 P4 P3 P2 P1 P0 | P7 P6 P5 P4 P3 P2 P1 P0 | |
| 3* | 16B1P1C | R7 R6 R5 R4 R3 G7 G6 G5 | G4 G3 G2 B7 B6 B5 B4 B3 | 8B1P1C | X X X X X X X X | P7 P6 P5 P4 P3 P2 P1 P0 | |
| 4* | 8B1P2C (4 + 4) | X X X X X X X X X X X X X X X X | X X X X P3 P2 P1 P0 X X X X P7 P6 P5 P4 | 24B1P2C | G7 G6 G5 G4 G3 G2 G1 G0 | B7 B6 B5 B4 B3 B2 B1 B0 R7 R6 R5 R4 R3 R2 R1 R0 | |
| 5* | 24B1P2C | G7 G6 G5 G4 G3 G2 G1 G0 | B7 B6 B5 B4 B3 B2 B1 B0 | 16B1P2C | X X X X X X X X X X X X X X X X | G4 G3 G2 B7 B6 B5 B4 B3 R7 R6 R5 R4 R3 G7 G6 G5 | |
| 6* | 16B1P2C | X X X X X X X X X X X X X X X X | G4 G3 G2 B7 B6 B5 B4 B3 R7 R6 R5 R4 R3 R2 R1 R0 | 24B1P2C | G7 G6 G5 G4 G3 G2 G1 G0 | B7 B6 B5 B4 B3 B2 B1 B0 R7 R6 R5 R4 R3 R2 R1 R0 | |
| 7* | 24B1P3C | X X X X X X X X X X X X X X X X | B7 B6 B5 B4 B3 B2 B1 B0 G7 G6 G5 G4 G3 G2 G1 G0 | 24B1P3C | X X X X X X X X X X X X X X X X | B7 B6 B5 B4 B3 B2 B1 B0 G7 G6 G5 G4 G3 G2 G1 G0 | |
| 8* | 8B1P2C (4 + 4) | X X X X X X X X X X X X X X X X | X X X X P3 P2 P1 P0 X X X X P7 P6 P5 P4 | 16B1P2C | X X X X X X X X X X X X X X X X | G4 G3 G2 B7 B6 B5 B4 B3 R7 R6 R5 R4 R3 G7 G6 G5 | |
| 9* | 8B1P2C (8 + 0) | X X X X X X X X X X X X X X X X | P7 P6 P5 P4 P3 P2 P1 P0 X X X X X X X X | 24B1P2C | G7 G6 G5 G4 G3 G2 G1 G0 | B7 B6 B5 B4 B3 B2 B1 B0 R7 R6 R5 R4 R3 R2 R1 R0 | |
| A† | 8B2P1C | P7 P6 P5 P4 P3 P2 P1 P0 | P7 P6 P5 P4 P3 P2 P1 P0 | 15B1P1C | X R7 R6 R5 R4 R3 G7 G6 | G5 G4 G3 B7 B6 B5 B4 B3 | |
| B† | 24B2P3C | G7 G6 G5 G4 G3 G2 G1 G0 B7 B6 B5 B4 B3 B2 B1 B0 R7 R6 R5 R4 R3 R2 R1 R0 | B7 B6 B5 B4 B3 B2 B1 B0 R7 R6 R5 R4 R3 R2 R1 R0 G7 G6 G5 G4 G3 G2 G1 G0 | 24B2P3C | G7 G6 G5 G4 G3 G2 G1 G0 B7 B6 B5 B4 B3 B2 B1 B0 R7 R6 R5 R4 R3 R2 R1 R0 | B7 B6 B5 B4 B3 B2 B1 B0 R7 R6 R5 R4 R3 R2 R1 R0 G7 G6 G5 G4 G3 G2 G1 G0 | |
| C | 15B1P2C | X X X X X X X X X X X X X X X X | G5 G4 G3 B7 B6 B5 B4 B3 X R7 R6 R5 R4 R3 G7 G6 | 8B1P2C (4 + 4) | X X X X X X X X X X X X X X X X | X X X X P3 P2 P1 P0 X X X X P7 P6 P5 P4 | |
| D† | 8B2P1C | P7 P6 P5 P4 P3 P2 P1 P0 | P7 P6 P5 P4 P3 P2 P1 P0 | 16B1P1C | R7 R6 R5 R4 R3 G7 G6 G5 | G4 G3 G2 B7 B6 B5 B4 B3 | |

Note: * = ATT20C498 compatible mode
 † = on-chip clock doubler enabled
 Bi, Gi, Ri = pixel input for bypass mode, where i indicates pixel bit number
 Pi = pixel input for pseudo-color mode, where i indicates pixel bit number
 X = unused bits

MIX-COLOR®

CH8398A offers an enhanced feature called MIX-COLOR® mode, which allows the simultaneous display of image regions with different spatial resolution and color depth in a single bitmapped frame. MIX-COLOR® is capable of displaying 64K colors within a high resolution (1280 x 1024 @ 75 Hz) graphics window. This feature is particularly useful in Windows® applications where a colorful picture is placed within a page of text.

Window Frame

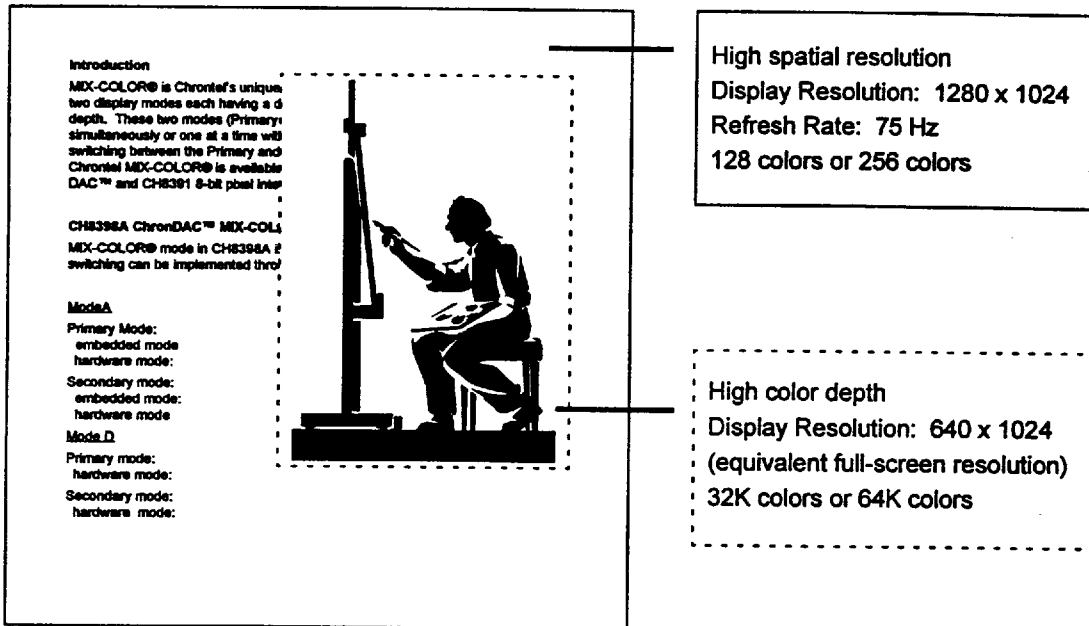


Figure 7: MIX-COLOR® Mode

MIX-COLOR® mode is available in modes A and D:

Mode A

| | | |
|-----------------|-------------------|------------|
| Primary mode: | Pseudo-color mode | |
| | embedded mode: | 128 colors |
| | hardware mode: | 256 colors |
| Secondary mode: | Bypass color mode | |
| | embedded mode: | 32K colors |
| | hardware mode: | 32K colors |

Mode D

| | | |
|-----------------|-------------------|------------|
| Primary mode: | Pseudo-color mode | |
| | hardware mode: | 256 colors |
| Secondary mode: | Bypass color mode | |
| | hardware mode: | 64K colors |

Comparison of MIX-COLOR® and PixMix™ Modes

CH8398A supports both MIX-COLOR® and PixMix™ modes for displaying high resolution graphics in addition to high color depth within the same frame of data.

MIX-COLOR®

- MIX-COLOR® has flexibility for both on-the-fly hardware and software (embedded) switching modes.
- MIX-COLOR® maintains the maximum possible resolution for the given clock rate by utilizing all pixel data available.
- 2 pixel addresses per pixel clock.
- MIX-COLOR® efficiently correlates pixel data stored in memory with pixel data displayed.
- MIX-COLOR® simultaneously displays bypass and pseudo-color modes with the following specs:
 - Bypass mode: 16-bit or 64K colors
 - Pseudo-color mode: 256 colors
 - Standard resolution (max): 1280 x 1024 @ 75 Hz

PixMix™

- PixMix™ implementation is only available in the embedded switching mode.
- PixMix™ pixel resolution does not fully utilize the pixel bus bandwidth or the frame buffer memory pixel data.
- 1 pixel address per pixel clock.
- PixMix™ inefficiently maps between pixel data stored in memory with pixel data displayed.
- PixMix™ simultaneously displays bypass and pseudo-color modes with the following specs:
 - Bypass mode: 15-bit or 32K colors
 - Pseudo-color mode: 256 colors
 - Standard resolution (max): 800 x 600 @ 72 Hz

Note: 1280 x 1024 can be achieved using Chrontel's MIX-COLOR®

Window Frame

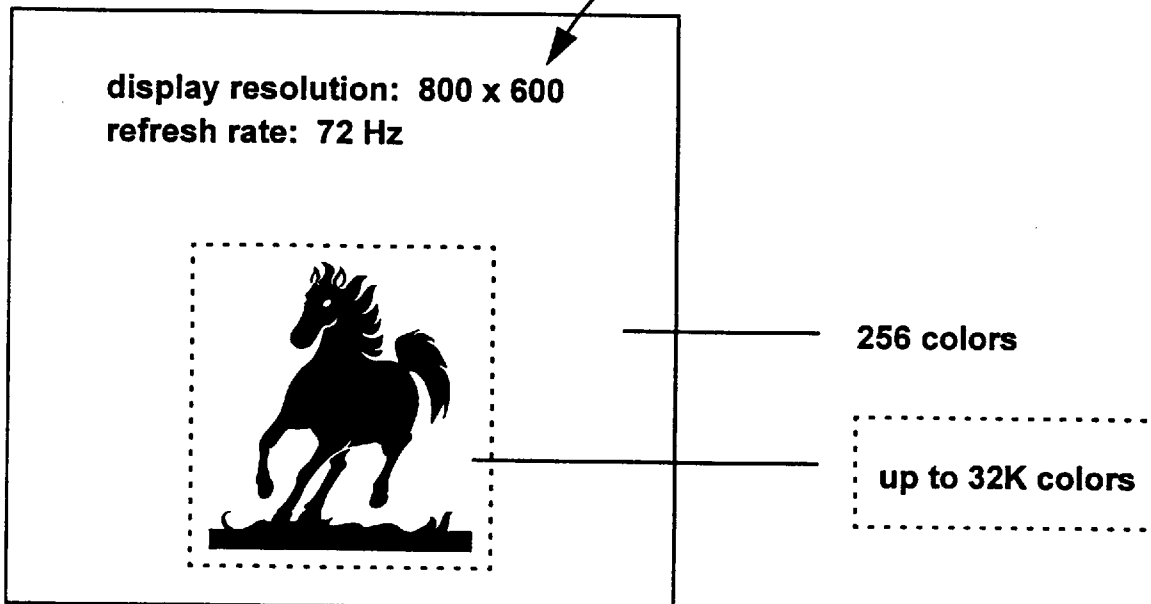


Figure 8: PixMix™ Mode

Examples of Embedded Mode Switching for MIX-COLOR® and PixMix™

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Example # 1: Embedded mode switching for MIX-COLOR®

Mode A

Primary mode: Pseudo-color mode
P[7] and P[15] set to 0

Secondary mode: Bypass color mode
P[15] set to 1

| | P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
|--------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| Pseudo | 0 | P6 | P5 | P4 | P3 | P2 | P1 | P0 | 0 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| 5-5-5 | 1 | R7 | R6 | R5 | R4 | R3 | G7 | G6 | G5 | G4 | G3 | B7 | B6 | B5 | B4 | B3 |

Note: Embedded case requires palette RAM table to be reconfigured for 128 colors instead of 256 colors

P[i] = pixel input pin

R[7:3] = red pixel data

G[7:3] = green pixel data

B[7:3] = blue pixel data

CH8398A is capable of implementing PixMix™ mode, using P[15] as a mode switch control signal.

Example # 2: Embedded mode switching for PixMix™

Mode 1

Primary mode: Bypass color mode
P[15] set to 0

Secondary mode: Pseudo-color mode
P[15] set to 1

| | P[15] | P[14] | P[13] | P[12] | P[11] | P[10] | P[9] | P[8] | P[7] | P[6] | P[5] | P[4] | P[3] | P[2] | P[1] | P[0] |
|--------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| 5-5-5 | 0 | R7 | R6 | R5 | R4 | R3 | G7 | G6 | G5 | G4 | G3 | B7 | B6 | B5 | B4 | B3 |
| Pseudo | 1 | X | X | X | X | X | X | X | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

Note: P[i] = pixel input pin

R[7:3] = red pixel data

P[7:0] = pseudo pixel address

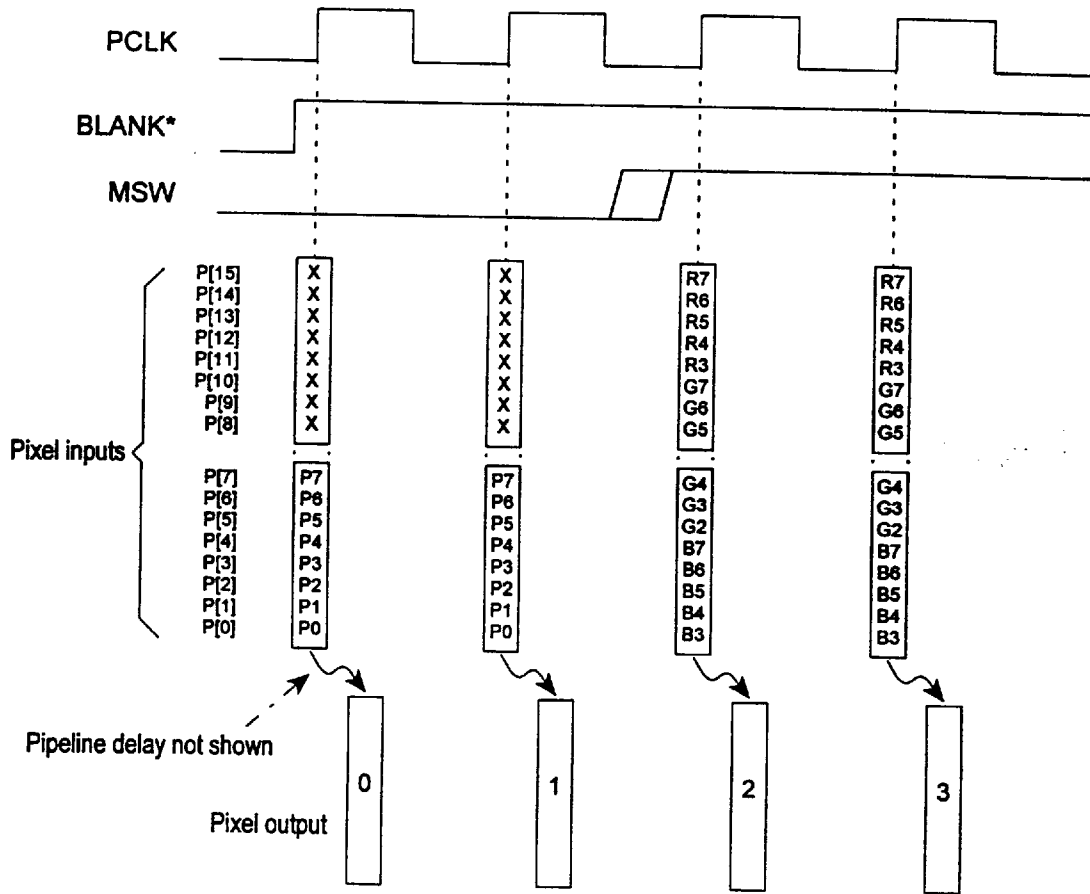
G[7:3] = green pixel data

X = unused bit

B[7:3] = blue pixel data

PCLK Timing Diagrams

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Primary mode: 8-bit bypass (8B1P1C)

Secondary mode: 16-bit bypass (16B1P1C)

Figure 9: PCLK Timing Mode 0 Using Hardware Mode Switching¹

| Mode | CR[7] | CR[6] | CR[5] | CR[4] | Primary Mode | Secondary Mode |
|------|-------|-------|-------|-------|--------------|---------------------|
| 0 | 0 | 0 | 0 | 0 | 8-bit pseudo | 16-bit 5-6-5 bypass |

Note: CR[7:4] corresponds to display mode control bits located in the control register

¹ Figures 9 through 12 represent the most commonly used options
For information on other available options, please call Chronitel

PCLK Timing Diagrams (continued)

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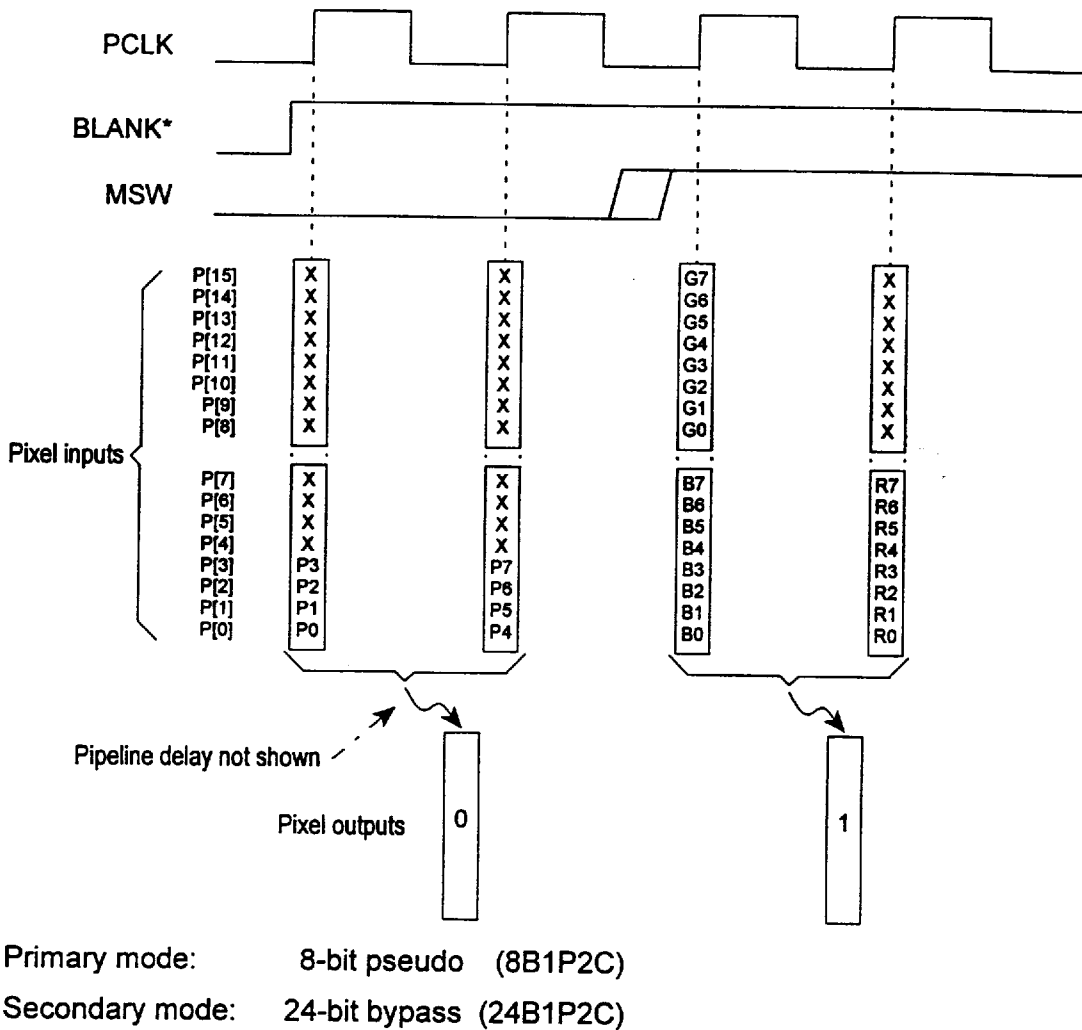


Figure 10: PCLK Timing for Mode 4 Using Hardware Mode Switching¹

| Mode | CR[7] | CR[6] | CR[5] | CR[4] | Primary Mode | Secondary Mode |
|------|-------|-------|-------|-------|--------------------|---------------------|
| 4 | 1 | 0 | 0 | 0 | 8-bit pseudo (4+4) | 24-bit 8-8-8 bypass |

Note: CR[7:4] corresponds to display mode control bits located in the control register

¹ Figures 9 through 12 represent the most commonly used options
For information on other available options, please call Chronitel

PCLK Timing Diagrams (continued)

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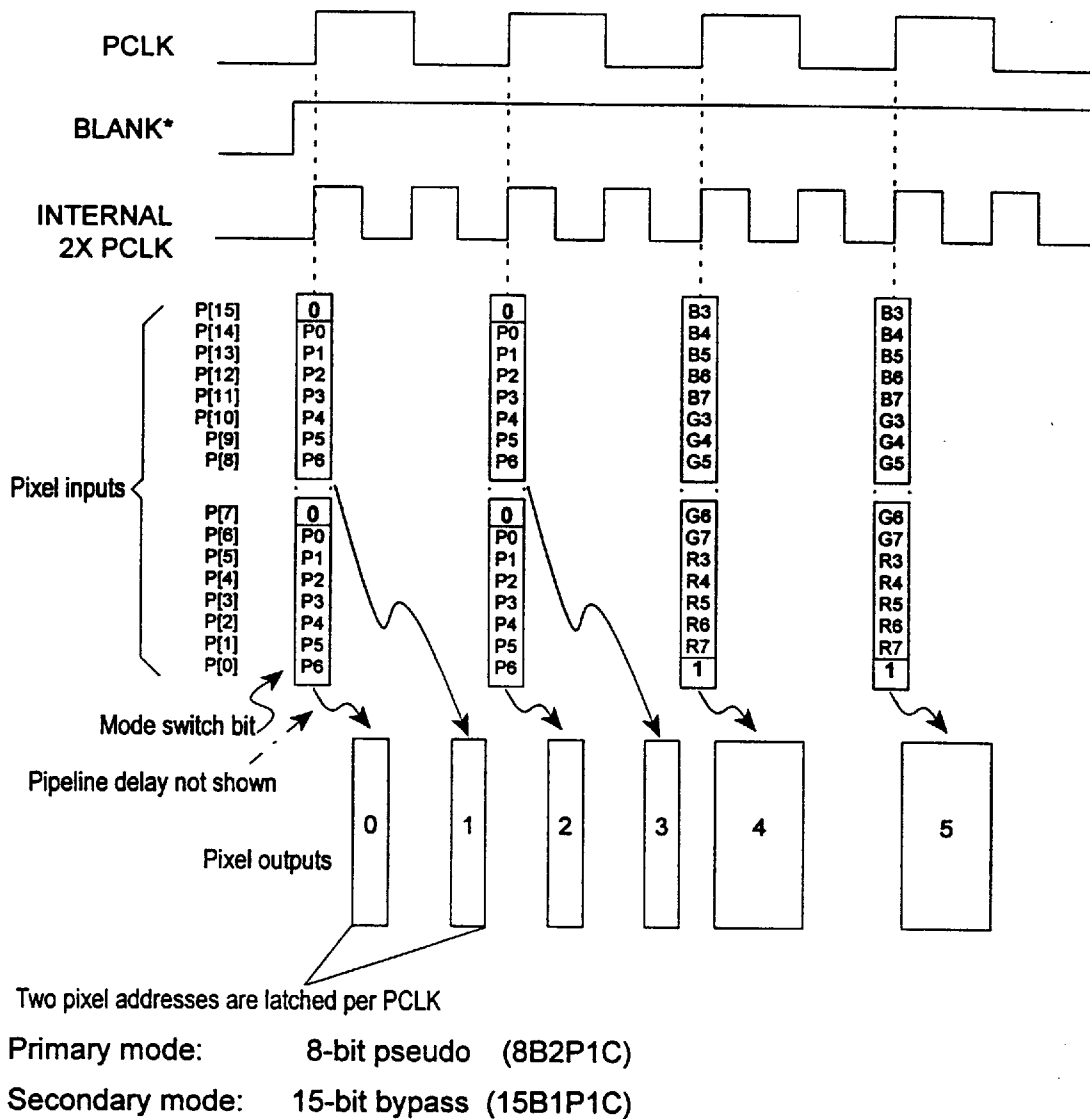


Figure 11: PCLK Timing for Mode A, MIX-COLOR®, Using Software Mode Switching¹

| Mode | CR[7] | CR[6] | CR[5] | CR[4] | Primary Mode | Secondary Mode |
|------|-------|-------|-------|-------|-------------------------|--------------------------------|
| A | 1 | 0 | 1 | 0 | MIX-COLOR® 8-bit pseudo | MIX-COLOR® 15-bit 5-5-5 bypass |

Note: CR[7:4] corresponds to display mode control bits located in the control register

¹ Figures 9 through 12 represent the most commonly used options
For information on other available options, please call Chromtel

PCLK Timing Diagrams (continued)

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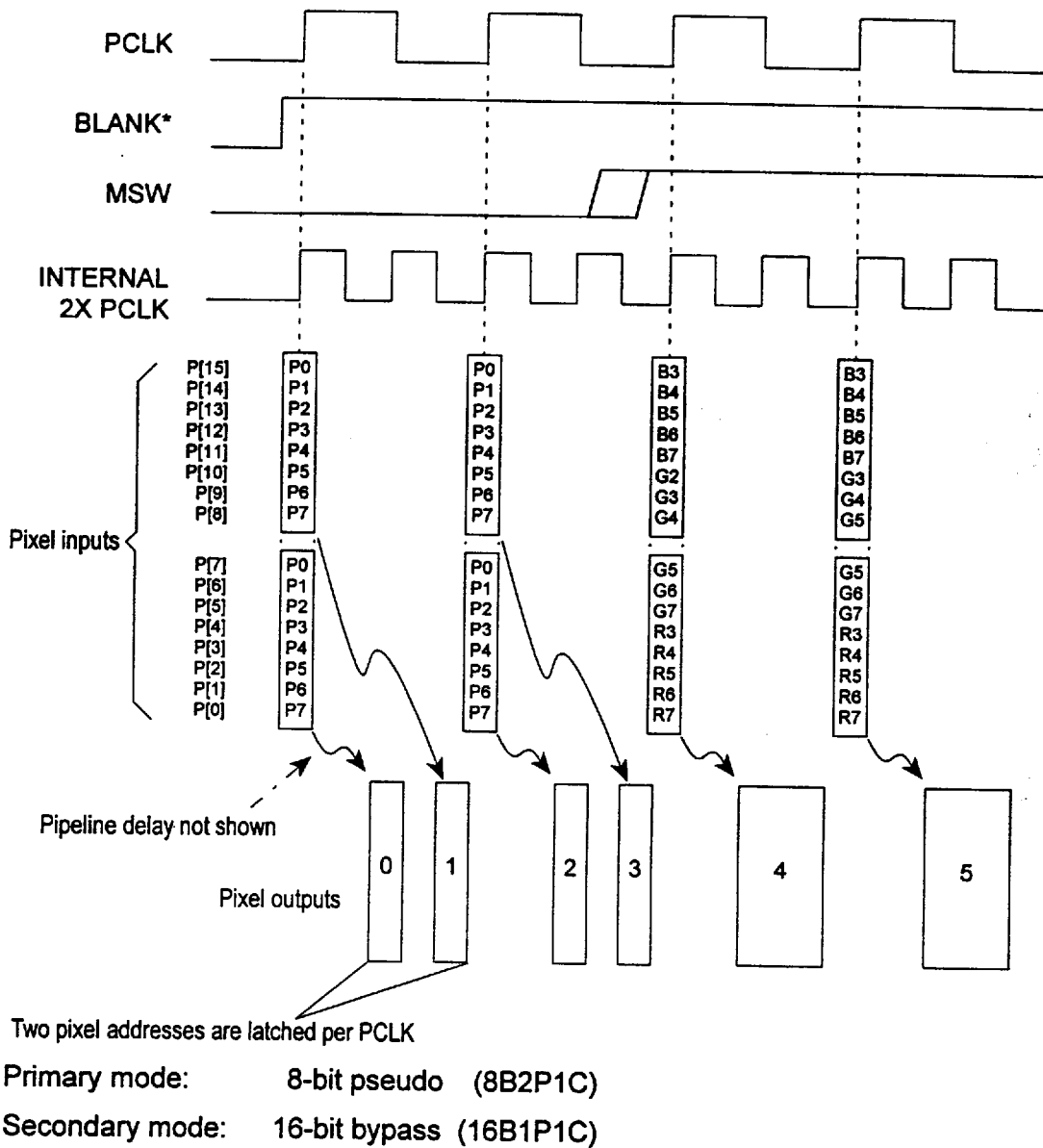


Figure 12: PCLK Timing for Mode D, MIX-COLOR®, Using Hardware Mode Switching¹

| Mode | CR[7] | CR[6] | CR[5] | CR[4] | Primary Mode | Secondary Mode |
|------|-------|-------|-------|-------|-------------------------|--------------------------------|
| D | 1 | 1 | 0 | 1 | MIX-COLOR® 8-bit pseudo | MIX-COLOR® 16-bit 5-6-5 bypass |

Note: CR[7:4] corresponds to display mode control bits located in the control register

¹ Figures 9 through 12 represent the most commonly used options
For information on other available options, please call Chronitel

Table 4 • Register Maps and Definitions

| | RS3 | RS2 | RS1 | RS0 | Description | Default upon Power Up |
|-------------------|-----|-----|-----|-----|--|-----------------------|
| PWA | 1 | 0 | 0 | 0 | Palette RAM Write Address Register | N/A |
| PDR | 1 | 0 | 0 | 1 | Palette RAM Data Register | N/A |
| RMR | 1 | 0 | 1 | 0 | Pixel Read Mask Register (IDR, alternate access to control register) | IDR = C0H CR = 00H |
| PRA | 1 | 0 | 1 | 1 | Palette RAM Read Address Register | N/A |
| CWA | 1 | 1 | 0 | 0 | Clock RAM Write Address Register (alternate access to clock select register) | N/A |
| CDR | 1 | 1 | 0 | 1 | Clock RAM Data Register | N/A |
| CR ¹ | 1 | 1 | 1 | 0 | Control Register | 00H |
| CRA | 1 | 1 | 1 | 1 | Clock RAM Read Address Register | N/A |
| CSR ¹ | 1 | 0 | 0 | 0 | Clock Select Register | 00H |
| IDR | — | — | — | — | Identification Register | C0H |
| TEST ¹ | 0 | 0 | 0 | 1 | Test Register (internal use only) | — |
| AUXR ² | — | — | — | — | Auxiliary Register | 00H |

Note: 1 These registers can also be accessed by using the alternate accessing method

2 This register can only be accessed by using the alternate accessing method

PWA: Palette RAM Write Address Register

PWA specifies the address to the palette RAM for write access.

PDR: Palette RAM Data Register

PDR contains the data read from the palette RAM or the data to be written to the RAM. The read address is specified by PRA, the write address is specified by PWA.

RMR: Read Mask Register

RMR is used in pseudo and MIX-COLOR® modes. Each bit of RMR is bit-wise logically “AND”ed with the 8-bit palette RAM address. The resulting address is used to point to the palette RAM. Under the alternate register access method, this register is used to access the ID Register, Control Register, Auxiliary Register, and Test Register. For further information, please refer to “Alternate Access Method” on page 37.

Note: This register is **NOT** initialized upon power up

When pseudo mode is activated, the pixel address uses the RMR. The RMR content is bit-wise “AND”ed with the pixel address, and the result is used to address the color palette RAM. On the 15-bit or 16-bit bypass mode, the lowest 2 or 3 bits of the DACs are padded with zeros. For further information, please refer to Figures 5 and 6 (page 20). In MIX-COLOR® mode, the masking operation is enabled for pseudo-color mode. To disable the masking operation, write FFH into the RMR.

PRA: Palette RAM Read Address Register

PRA specifies the address to the palette RAM for read access.

CWA: PLL Clock RAM Write Address Register

CWA specifies the address to the PLL RAM for write access. Using the alternate register access, CWA accesses the Clock Select Register. For further information, please refer to “Alternate Access Method” on page 37.

CDR: PLL Clock RAM Data Register

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CDR contains data read from the PLL RAM or data to be written to the RAM. CRA specifies the read address and CWA specifies the write address.

CR: Control Register

CR determines the display modes, power down modes, and MPU interface to the color palette RAM.

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CR[7] | CR[6] | CR[5] | CR[4] | CR[3] | CR[2] | CR[1] | CR[0] |
| DM3 | DM2 | DM1 | DM0 | PD1 | MSDIS | V / P | PD0 |

CR[0]:PD0 = Power Down control bit 0

These power down modes are well-suited for both LCD and CRT applications, and support "Green PC" applications. CH8398A supports both LCD graphics-only controllers and LCD graphics controllers with simultaneous CRT and LCD display. Power consumption of the graphics subsystem can be greatly reduced using these power down modes.

CR[1]:V / P = Select VCLK / PCLK ratio

If:

the MNK values of VCLK are chosen so $VCLK / PCLK = 1$,

then:

set $CR[1] = 0$

This is used only for optimization of the internal doubler.

Please note that whether CR[1] is set to "0" or "1," a change may not be readily apparent to the user.

For example: PCLK = 28.322 MHz, and the VGA controller requires
 $VCLK = 2 \times PCLK$

Step 1. Program the proper M, N, and K values in the PLL RAM to generate 56.444 MHz (i.e., M = 21, N = 174, K = 1)

Step 2. Set $CR[1] = 1$

This example requires the following data format:

| MSB | | | | | | | | LSB | | | | | | | |
|-----|----|----|----|----|----|----|----|-----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |

CR[2]: MSDIS = MSW input pin disable

0 = MSW pin control display mode switching (default)

1 = MSW pin in interpreted as 0 regardless of its state

CR[3]: PD1 = Power Down control bit 1

CR: Control Register (continued)

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Table 5 • Power Down Control Bits.

| CR[3] | CR[0] | Description |
|-------|-------|--|
| PD1 | PD0 | |
| 0 | 0 | MPLL, VPLL, and LUTDAC are ON. Normal operation mode. |
| 0 | 1 | MPLL and VPLL are ON, LUTDAC is OFF. Used for flat panel controller where LUTDAC is not required. Both PLL and palette RAMs can still be accessed from the MPU bus. |
| 1 | 0 | MPLL is ON, VPLL and LUTDAC are OFF. MPLL is on, memory image is retained. Used in CRT and flat panel applications. Both PLL and palette RAMS can still be accessed from the MPU bus. |
| 1 | 1 | MPLL, VPLL and LUTDAC are OFF. Graphics subsystem is completely powered down. Only palette RAM can still be accessed from the MPU bus. |

CR[7:4]: Display mode control bits

These bits correspond to DM[3:0] in the control register are used to select the display modes.

Table 6 • Display Mode Control Bits

| Mode | CR[7] | CR[6] | CR[5] | CR[4] | Description | |
|------|-------|-------|-------|-------|--------------------------|---------------------------------|
| | DM3 | DM2 | DM1 | DM0 | MSW = 0, PRIMARY MODE | MSW = 1, SECONDARY MODE |
| 0* | 0 | 0 | 0 | 0 | 8-bit pseudo | 16-bit 5-6-5 bypass |
| 1* | 0 | 0 | 0 | 1 | 15-bit 5-5-5 bypass | 8-bit pseudo |
| 2† | 0 | 0 | 1 | 0 | 8-bit pseudo | 8-bit pseudo |
| 3* | 0 | 0 | 1 | 1 | 16-bit 5-6-5 bypass | 8-bit pseudo |
| 4* | 0 | 1 | 0 | 0 | 8-bit pseudo (4 + 4) | 24-bit 8-8-8 bypass |
| 5* | 0 | 1 | 0 | 1 | 24-bit 8-8-8 bypass | 16-bit 5-6-5 bypass |
| 6* | 0 | 1 | 1 | 0 | 16-bit 5-6-5 bypass | 24-bit 8-8-8 bypass |
| 7* | 0 | 1 | 1 | 1 | 24-bit 8-8-8 bypass | 24-bit 8-8-8 bypass |
| 8* | 1 | 0 | 0 | 0 | 8-bit pseudo (4 + 4) | 16-bit 5-6-5 bypass |
| 9* | 1 | 0 | 0 | 1 | 8-bit pseudo (8 + 0) | 24-bit 8-8-8 bypass |
| A† | 1 | 0 | 1 | 0 | MIX-COLOR®, 8-bit pseudo | MIX-COLOR®, 15-bit 5-5-5 bypass |
| B† | 1 | 0 | 1 | 1 | 24-bit 8-8-8 bypass | 24-bit 8-8-8 bypass |
| C | 1 | 1 | 0 | 0 | 15-bit 5-5-5 bypass | 8-bit pseudo (4 + 4) |
| D† | 1 | 1 | 0 | 1 | MIX-COLOR®, 8-bit pseudo | MIX-COLOR®, 16-bit 5-6-5 bypass |

Note: * = ATT20C498 compatible mode

† = on-chip clock doubler enabled

CRA: PLL Clock RAM Read Address Register

CRA specifies the address to the PLL RAM for read access.

CSR:Clock Select Register

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CSR internally selects MPLL and VPLL frequencies. See Table 11 on page 40 for further details on PLL RAM data organization.

CSR[3:0]: VS[3:0] = VPLL Select

These bits are logically bit-wise "OR"ed with the external FS[3:0].
Selects 1 of 16 entries.

CSR[6:4]: MS[2:0] = MPLL Select

Selects 1 of 8 entries.

CSR[7]: PH* = PLL Frequency Hold

CSR[7] = 0 PLL frequency holds at the current value. No change to MCLK or VCLK outputs, regardless of the value written to CSR[6:0] of this register, or the state of external FS[3:0].

CSR[7] = 1 PLL frequency releases the current value. MCLK frequency depends on the value of MS[2:0] (CSR[6:4]). VCLK frequency depends on the logically bit-wise "OR"ed value of external FS[3:0] with the internal VS[3:0] (CSR[3:0]).

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| CSR[7] | CSR[6] | CSR[5] | CSR[4] | CSR[3] | CSR[2] | CSR[1] | CSR[0] |
| PH* | MS2 | MS1 | MS0 | VS3 | VS2 | VS1 | VS0 |

IDR: Identification Register

IDR is a read only register with a predefined value of C0H.

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| IDR[7] | IDR[6] | IDR[5] | IDR[4] | IDR[3] | IDR[2] | IDR[1] | IDR[0] |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

TEST: Test Register

TEST is for internal use only.

AUXR: Auxiliary Register

AUXR sets both the video and memory clock output voltage levels to a target 50% duty cycle. See Tables 7 and 8 page 33 for available voltage levels.

AUXR[1:0]: VL[1:0] = Select bits for video clock voltage level output

AUXR[3:2]: ML[1:0] = Select bits for memory clock voltage level output

AUXR[4]: Reserved bit

AUXR[5]: = 0 frequency doubler enabling base on Color Mode selection
(it is recommended AUXR[5] be set to 0)

= 1 frequency doubler enabled (independent of Color Mode)

AUXR[6]: = 0 normal operation

= 1 invert MSW

AUXR: Auxiliary Register (continued)

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AUXR[7] used to eliminate requirement of RS2 pin
 If RS2 pin is used, then the user should keep AUXR[7] = 0 and RS[2:0] will be decoded as specified in Table 4, "Register Maps and Definitions," on page 29.
 If RS2 pin is not used (i.e., RS2 pin connects to GND permanently), AUXR[7] can be used to change the mapping, as shown below.

| | AUXR[7] = 0 | AUXR[7] = 1 |
|-----|-------------|-------------|
| 3C7 | PRA | CRA |
| 3C8 | PWA | CWA |
| 3C9 | PDR | CDR |

In summary, when
 AUXR[7] = 0 normal operation
 (access Color RAM related hardware when RS2 = 0
 access PLL-Ram related hardware when RS2 = 1)
 = 1 access PLL-RAM related hardware

Table 7 • Video Clock

| AUXR[1] | AUXR[0] | Targeted 50% Duty Cycle |
|---------|---------|-------------------------|
| VL1 | VL0 | Level (Volts) |
| 0 | 0 | 1.8 |
| 0 | 1 | 1.5 |
| 1 | 0 | 2.1 |
| 1 | 1 | 2.4 |

Table 8 • Memory Clock

| AUXR[3] | AUXR[2] | Targeted 50% Duty Cycle |
|---------|---------|-------------------------|
| ML1 | ML0 | Level (Volts) |
| 0 | 0 | 1.8 |
| 0 | 1 | 1.5 |
| 1 | 0 | 2.1 |
| 1 | 1 | 2.4 |

MPU Access

All MPU access is through D[7:0] bus, with RD* and WR* control signals, and RS[3:0] to select which register is to be accessed. Some registers have an alternate access method for graphics controllers that do not provide an RS3 output signal.

Access to the Palette RAM

6-bit Access to the Palette RAM

CH8398A supports access to the Palette RAM only in a 6-bit format, as indicated in Figures 13 and 14 below.

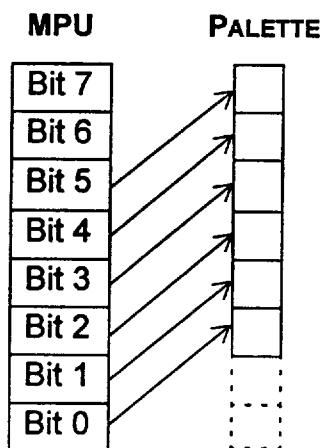


Figure 13: 6-bit Write Mode

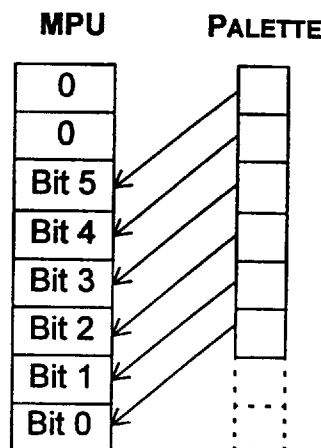


Figure 14: 6-bit Read Mode

To write the palette RAM:

- Step 1. Load the initial RAM write address to PWA.
- Step 2. Write PDR with the red, green, and blue values. The first write is accessed to write the data to be stored in the red temporary register, the second is the green, and the third is the blue. Internally there is a modulo 3 counter. After the third (blue) write to the PDR, the red, green, and blue data is written to the palette RAM and the address is incremented. The entire palette RAM can be written by sequential writes to PDR. The address rolls over to 00H after reaching FFH. The modulo 3 counter resets after each write to PRA or PWA.

To read the palette RAM:

- Step 1. Load the initial RAM read address to PRA. This action triggers a fetch from the palette RAM, transferring the red, green, and blue data to the temporary register. The address is automatically incremented after the fetch.
- Step 2. Read the PDR for the red, green, and blue values. The first read is accessed to read the data stored in the red temporary register, the second to green, and the third to blue. Internally there is a modulo 3 counter. After the third (blue) access, the device triggers another fetch followed by an address increment. The entire palette RAM can be read by sequential reads of the PDR. The address rolls over to 00H after reaching FFH. The modulo 3 counter resets after each write to PRA or PWA.

Table 9 • Palette RAM Data Organization

| Address | Byte 0 | Byte 1 | Byte 2 |
|---------|--------|--------|--------|
| 00H | Red | Green | Blue |
| 01H | Red | Green | Blue |
| ... | ... | ... | ... |
| ... | ... | ... | ... |
| ... | ... | ... | ... |
| FEH | Red | Green | Blue |
| FFH | Red | Green | Blue |

Access to the PLL Clock RAM

Access to PLL Clock RAM is similar to the palette RAM, except the modulus counter is modulo 2. Each PLL is two bytes wide: the first access is the LSB, the second is the MSB value. VPLL has 16 locations, occupying the first 32 bytes, while MPLL occupies the next 16 bytes with 8 locations.

To write the PLL Clock RAM:

- Step 1. Load the initial RAM write address to the CWA.
- Step 2. Write CDR with the PLL values. The first write is the LSB, the second is the MSB. After the MSB write, the PLL data is written to the PLL RAM and the address is incremented. The entire PLL RAM can be written by sequential writes to CDR. The internal modulo 2 counter resets after each write to the CRA or CWA.

To read the PLL Clock RAM:

- Step 1. Load the initial RAM read address to the CRA. This triggers a fetch from the PLL Clock RAM, and the data transfers to the temporary register. The address automatically increments after the fetch.
- Step 2. Read the CDR for the PLL values. The first read is the access to the LSB, the second is the MSB. After the MSB access, the device triggers another fetch followed by an address increment. The entire PLL RAM can be read by sequential reads of the CDR. The internal modulo 2 counter resets after each write to CRA or CWA.

Table 10 • PLL Clock RAM Data Organization

| Address Location | Frequency Outputs (MHz) | CSR[6:4] MS[2:0] | CSR[3:0] ¹ VS[3:0] |
|------------------|-------------------------|------------------|-------------------------------|
| 00H | 25.175 | N/A | 0H |
| 01H | 28.322 | N/A | 1H |
| ... | VPLL | ... | ... |
| 0FH | VPLL | N/A | FH |
| 10H | MPLL | 0H | N/A |
| ... | MPLL | ... | ... |
| 17H | MPLL | 7H | N/A |

Note: 1 CSR[3:0] is logically bit-wise “OR”ed with external FS[3:0] inputs respectively

Locations 0 – 1 of the VPLL RAM, providing the following frequencies, are initialized but may be overwritten:

- Location 0 VCLK = 25.175 MHz
- Location 1 VCLK = 28.322 MHz

Alternate Access Method

CH8398A offers an alternate method to access several registers. This method is designed for graphics controllers that do not use an RS3 signal.

The alternate access method applies to the following registers:

- CSR
- CR
- IDR
- AUXR

Note: The AUXR register can only be accessed through the alternate access method. CR can be accessed without using the alternate access method even though the RS3 signal from the graphics controller is not used.

Access to the Clock Select Register

There are two methods of accessing the CSR. The first method requires RS[3:0] to be driven to [0000]. The alternate method does not require the RS3 signal. With RS3 internally pulled high, alternate access to CSR is achieved by:

- Step 1. Set RS[2:0] to [100].
- Step 2. Read CWA four consecutive times without accessing any other register between reads.
- Step 3. The fifth access (read or write) is directed to the CSR. Only one access is allowed for each sequence. During the alternate access sequence, RS[2:0] must be set to [100]. To terminate the access sequence, access a register other than the CWA.

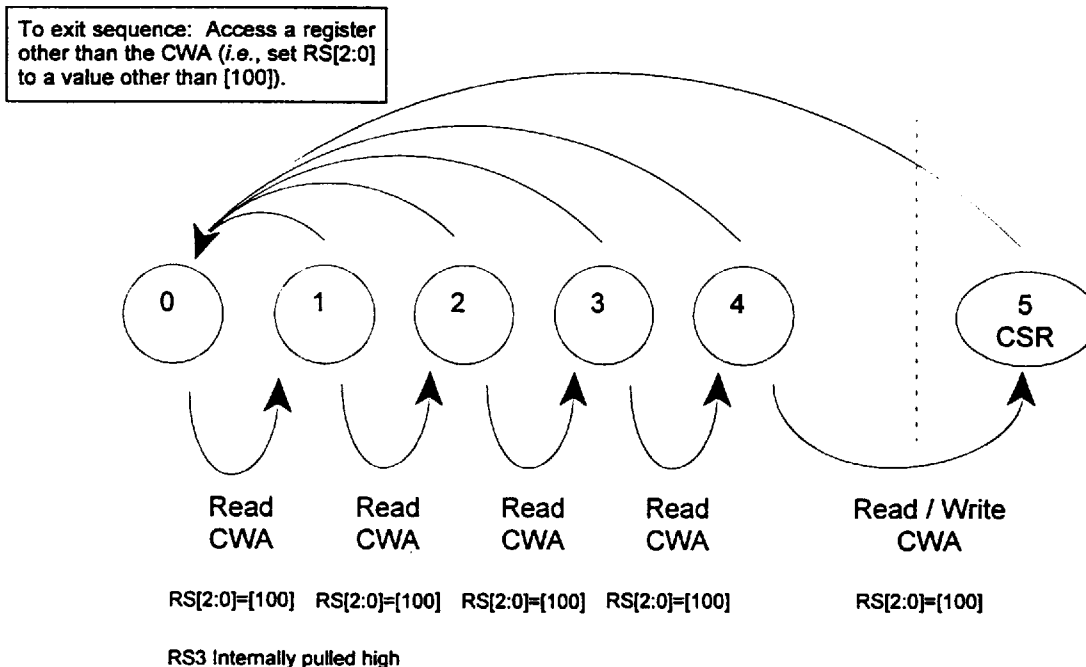


Figure 15: State for Alternate Access to Clock Select Register

Alternate Access Method (continued)

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Access to the Control Register

There are two ways of accessing the CR. The first method requires RS[2:0] to be driven to [110]. The alternate method does not require the RS3 signal. With RS3 internally pulled high, alternate access to CR is achieved by:

- Step 1. Set RS[2:0] to [010].
- Step 2. Read RMR four consecutive times, without accessing any other register between reads. Please note the fourth read access returns the value of the IDR.
- Step 3. The fifth access (read or write) is directed to the CR. Only one access is allowed for each sequence. During the alternate access sequence, RS[2:0] must be set to [010]. The sequence will terminate and return to its initial state at any point when the content of RS[2:0] ≠ [010].

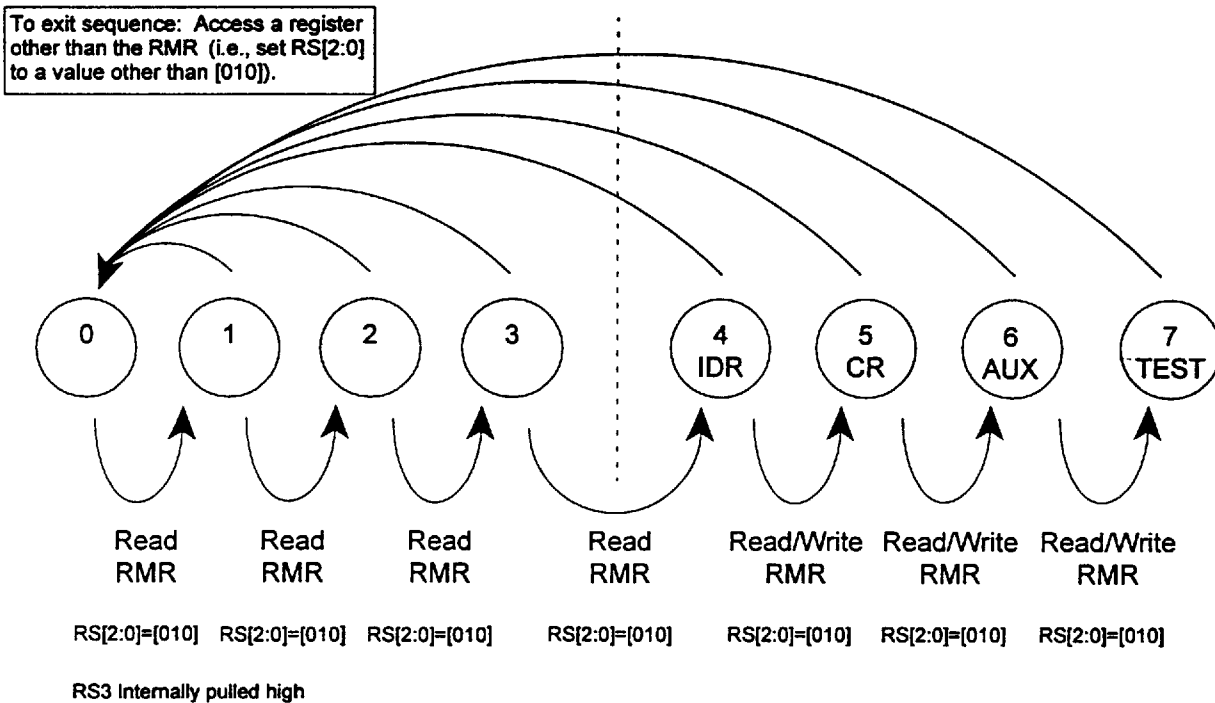


Figure 16: State for Alternate Access to ID, Control, Auxiliary, and Test Registers

Access to the Identification Register

Access to the IDR is achieved by:

- Step 1. Set RS[2:0] to [010].
- Step 2. Read the RMR three consecutive times, without accessing any other register between reads.
- Step 3. The fourth read returns the content of the IDR. Only one access is allowed for each sequence. During the alternate access sequence, RS[2:0] must be set to [010]. The sequence will terminate and return to its initial state at any point when the content of RS[2:0] ≠ [010].

Alternate Access Method (continued)

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Access to the Auxiliary Register

Access to AUXR is achieved by:

- Step 1. Set RS[2:0] to [010].
- Step 2. Read RMR four consecutive times, without accessing any other register between reads. Please note the fourth read access returns the value of the IDR, and the fifth access (read or write) is directed to the CR.
- Step 3. The sixth access (read or write) is directed to AUXR. Only one access is allowed for each sequence. During the alternate access sequence, RS[2:0] must be set to [010]. The sequence will terminate and return to its initial state at any point when the content of RS[2:0] ≠ [010]. Writing 00H to the next access will also terminate the sequence.

PLL Clock Generator

CH8398A incorporates Chronitel's proprietary PLL technology, which is capable of generating any frequency from 8 MHz – 135 MHz, by writing the appropriate values to the PLL RAM. To synthesize various frequencies used in different graphics modes, a stable reference frequency is required. The source of this reference frequency can come from either:

- an on-chip crystal oscillator (a crystal with a nominal frequency of 14.318 MHz is required between pins 6 and 7), *or*
- an external frequency source being applied to pin 7 of CH8398A with pin 6 grounded.

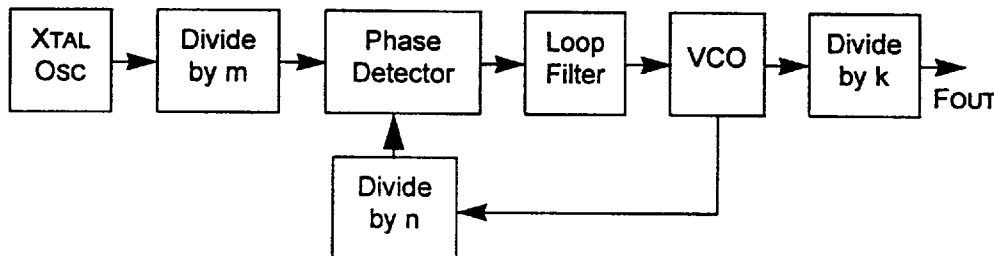


Figure 17: PLL Block Diagram

The formula for calculating the output frequency is achieved by:

$$F_{OUT} = F_{REF} \times \frac{n}{m \times k}$$

where:

- FREF = 14.318 MHz (for normal operation)
- m = M + 2
- n = N + 8
- k = 2^K

| MSB | | | | | | | | LSB | | | | | | | |
|-----|----|----|----|----|----|----|----|-----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| K1 | K0 | M5 | M4 | M3 | M2 | M1 | M0 | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 |

Note: Table 11 on page 40 shows some samples of M, N, and K values to be programmed. For frequencies not listed below, please contact Chronitel.

D[7:0] = data bus input from graphics controller
M[5:0] = reference frequency input divider

K[1:0] = output frequency scale
N[7:0] = VCO frequency divider

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Table 11 • Sample Frequency Coefficients (reference frequency = 14.318 MHz)

| FOUT | M | N | K |
|--------|----|-----|---|
| 14.318 | 8 | 72 | 3 |
| 25.06 | 3 | 27 | 2 |
| 25.20 | 23 | 168 | 2 |
| 25.95 | 6 | 50 | 2 |
| 27.44 | 7 | 61 | 2 |
| 28.28 | 8 | 71 | 2 |
| 28.33 | 21 | 174 | 2 |
| 28.64 | 2 | 24 | 2 |
| 30.07 | 3 | 34 | 2 |
| 31.50 | 8 | 80 | 2 |
| 32.57 | 8 | 83 | 2 |
| 33.75 | 5 | 58 | 2 |
| 35.89 | 3 | 17 | 1 |
| 37.59 | 6 | 34 | 1 |
| 38.48 | 6 | 35 | 1 |
| 40.09 | 8 | 48 | 1 |
| 43.98 | 5 | 35 | 1 |
| 44.74 | 6 | 42 | 1 |
| 47.25 | 3 | 25 | 1 |
| 50.11 | 3 | 27 | 1 |
| 51.90 | 6 | 50 | 1 |
| 54.89 | 7 | 61 | 1 |

| FOUT | M | N | K |
|--------|---|----|---|
| 56.56 | 8 | 71 | 1 |
| 57.27 | 2 | 24 | 1 |
| 60.14 | 3 | 34 | 1 |
| 63.00 | 8 | 80 | 1 |
| 65.15 | 8 | 83 | 1 |
| 67.50 | 5 | 58 | 1 |
| 71.59 | 3 | 17 | 0 |
| 75.17 | 6 | 34 | 0 |
| 76.96 | 6 | 35 | 0 |
| 80.18 | 8 | 48 | 0 |
| 87.95 | 5 | 35 | 0 |
| 89.49 | 6 | 42 | 0 |
| 94.50 | 3 | 25 | 0 |
| 100.23 | 4 | 34 | 0 |
| 105.00 | 7 | 58 | 0 |
| 108.18 | 7 | 60 | 0 |
| 109.77 | 7 | 61 | 0 |
| 118.12 | 2 | 25 | 0 |
| 120.27 | 3 | 34 | 0 |
| 130.91 | 5 | 56 | 0 |
| 135.00 | 5 | 58 | 0 |

Note: Use M values of 10 or less for best circuit performance

Electrical Specifications

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Table 12 • Absolute Maximum Ratings

| Symbol | Description | Min | Typ | Max | Units |
|--------|--|-----------|-----|------------|-------|
| | VDD relative to GND | -0.5 | | 7.0 | V |
| | Input voltage of all digital pins ¹ | GND - 0.5 | | VDD + 0.5 | V |
| | Analog output short circuit duration | | | Indefinite | Sec |
| TSTOR | Storage temperature | -65 | | 150 | °C |
| TJ | Junction temperature | | | 150 | °C |
| TvPS | Vapor phase soldering (one minute) | | | 220 | °C |

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

- The device is fabricated using high-performance CMOS technology. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5V can induce destructive latchup.

Table 13 • Recommended Operating Conditions

| Symbol | Description | Min | Typ | Max | Units |
|--------|---|--------------|----------------|----------------|----------|
| VDD | Supply voltage | 4.75 | 5.00 | 5.25 | V |
| TA | Ambient operating temperature | 0 | 25 | 70 | °C |
| RL | Output load to DAC outputs | | 37.5 | | Ω |
| IREF | Reference current RS-343A output PS/2™ compatible | -3.0 -3.0 | -8.39 -8.88 | -10.0 -10.0 | mA mA |

Table 14 • DC Characteristics (Operating Conditions: TA = 0°C – 70°C, VDD = 5V ± 5%)

| Symbol | Description | Test Condition @TA = 25°C | Min | Typ | Max | Unit |
|--------|------------------------------|---------------------------|-----|-----|-----|------|
| | Resolution (each DAC) | | 8 | 8 | 8 | Bits |
| | Accuracy (each DAC) | | | | | |
| LI | Integral linearity error | | | | ±1 | LSB |
| LD | Differential linearity error | | | | ±1 | LSB |
| | Gray scale error | | | | ±5 | % |
| | Monotonicity | Guaranteed | | | | |
| | Coding | Binary | | | | |

Table 15 • Digital Inputs / Outputs

| Symbol | Description | Test Condition @ TA = 25°C | Min | Typ | Max | Units |
|--------|---|----------------------------|-----------|-----|-----------|-------|
| VOH | Output high voltage | IOH = -400µA | 2.4 | | | V |
| VOL | Output low voltage | IOL = 3.2 mA | | | 0.4 | V |
| VIH | Input high voltage | | 2.0 | | VDD + 0.5 | V |
| VIL | Input low voltage | | GND - 0.5 | | 0.8 | V |
| ILK | Input leakage current (except for FS[3:0]) | | -10 | | 10 | µA |
| IPLD | Input pull down current FS[3:0] | VIN = 0.5V | | | 20 | µA |
| CDIN | Input capacitance (except for XI, XO / FIN) | f = 1 MHz, VIN = 2.4V | | | 7 | pF |
| CDIN | Input capacitance (XI, XO / FIN) | f = 1 MHz, VIN = 2.4V | | 20 | | pF |
| IOZ | Tri-state current | | | | 50 | µA |
| CDOUT | Output capacitance | | | | 7 | pF |

Table 16 • Clock Output Buffer

| Symbol | Description | Test Condition @ TA = 25°C | Min | Typ | Max | Units |
|--------|---------------------|----------------------------|-----|-----|-----|-------|
| IOH | Output high current | VOUT = 2.4V | -8 | | | mA |
| IOL | Output low current | VOUT = 0.5V | 8 | | | mA |

Table 17 • Analog Outputs (Operating Conditions: TA = 0°C – 70°C, VDD = 5V ± 5%)

| Symbol | Description | Test Condition @ TA = 25°C | Min | Typ | Max | Units |
|--------|---|----------------------------|-------|-------|-------|-----------|
| IGRAY | Gray scale current range | | | | 20 | mA |
| IWB | White level relative to black RS-343A PS/2™ | VREF = 1.23V | 16.74 | 17.62 | 18.50 | mA |
| | | RSET = 147 Ω | 18.00 | 18.65 | 20.00 | mA |
| | Black level relative to blank | | | 0 | | mA |
| IBLNK | Blank level | | | 0 | | mA |
| | DAC-to-DAC matching | | | 2 | 5 | % |
| VOC | Output compliance | | -1.0 | | +1.5 | V |
| ZAOUT | Output impedance | | | 10 | | kΩ |
| CAOUT | Output capacitance | f = 1 MHz, IOUT = 0 mA | | | 30 | pF |
| IVREF | Voltage reference input current | | | 10 | | µA |
| PSRR | Power supply rejection ratio | | | | 0.5 | % / % VDD |

Table 18 • AC Characteristics

| Symbol | Description | 110 | 135 | Units |
|----------------------------------|--|---------------|---------------|----------------------------|
| F_MAX | Single-edge data clock rate | 110 | 135 | MHz |
| F_MAX | Dual-edge data clock rate | 110 | 135 | MHz |
| t1_MIN | RS[3:0] setup time | 10 | 10 | ns |
| t2_MIN | RS[3:0] hold time | 10 | 10 | ns |
| t3_MIN | RD* active to data asserted | 5 | 5 | ns |
| t4_MAX | RD* active to data valid | 30 | 30 | ns |
| t5_MAX | RD* inactive to data tristated | 15 | 15 | ns |
| t6_MIN | Read data hold time | 5 | 5 | ns |
| t7_MIN | Write data setup time | 10 | 10 | ns |
| t8_MIN | Write data hold time | 10 | 10 | ns |
| t9_MIN | RD*, WR* low pulse width | 50 | 50 | ns |
| t10_MIN | RD*, WR* high pulse width | 7 | 7 | PCLK cycles |
| t11_MIN | Pixel input setup time | 2 | 2 | ns |
| t12_MIN | Pixel input hold time | 2 | 2 | ns |
| t11_MIN | BLANK* setup time | 2 | 2 | ns |
| t12_MIN | BLANK* hold time | 2 | 2 | ns |
| t11_MIN | MSW setup time | 2 | 2 | ns |
| t12_MIN | MSW hold time | 2 | 2 | ns |
| t13_MIN | Clock cycle time | 9.09 | 7.4 | ns |
| t14_MIN | Clock pulse width high | 3.5 | 3 | ns |
| t15_MIN | Clock pulse width low | 3.5 | 3 | ns |
| t16_MAX | Analog output delay | 30 | 30 | ns |
| t17_TYP | Analog output rise / fall time | 2 | 2 | ns |
| t18_MAX | Analog output settling time | 9 | 7.4 | ns |
| TSU_MIN | Setup time, data to strobe | 5 | 5 | ns |
| THOLD_MIN | Hold time, strobe to data | 5 | 5 | ns |
| TSTROBE_MIN | Strobe pulse width | 20 | 20 | ns |
| TYP | Glitch impulse energy ¹ | 75 | 75 | pV – sec |
| TYP | DAC-to-DAC crosstalk | -23 | -23 | dB |
| MAX | Analog output skew | 2 | 1.5 | ns |
| MIN MAX | Pipeline delay | 6 9 | 6 9 | PCLK cycles PCLK cycles |
| IDD_TYP | VDD supply current ¹ | 180 | 200 | mA |
| IPD1_TYP IPD2_TYP IPD3_TYP | Power down mode ¹ Mode 1: MPLL & VPLL ON, LUTDAC OFF Mode 2: MPLL ON, VPLL & LUTDAC OFF Mode 3: MPLL, VPLL, & LUTDAC OFF | 55 35 2 | 55 35 2 | mA mA mA |

Note: 1 MCLK = 40 MHz and VCLK = 28.32 MHz

Test Conditions: Unless otherwise specified, the testing conditions are the same as in Table 13, "Recommended Operating Conditions," on page 41. TTL input values are 0 – 3V, with input rise / fall times < 3 ns, measured between the VIL and VIH. Timing reference points at 50% for non-TTL inputs and outputs. TTL reference points at 1.5V for inputs and outputs. Analog output load < 10 pF, D[7:0] output load < 45 pF

Timing Diagrams

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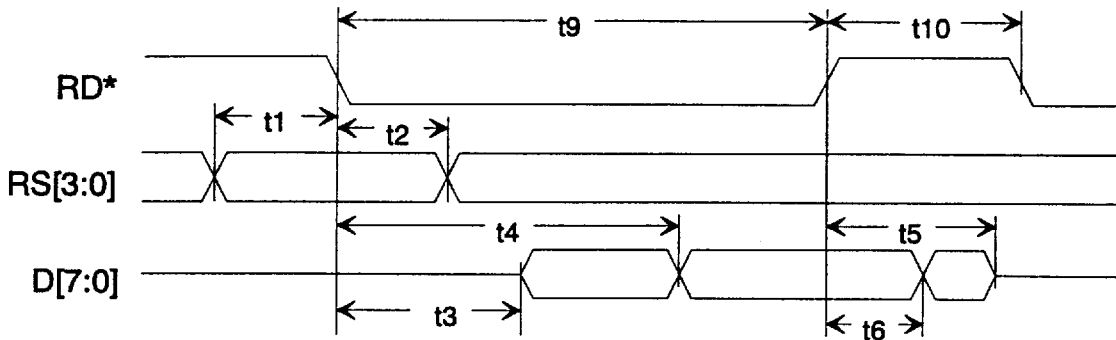


Figure 18: MPU Read Timing

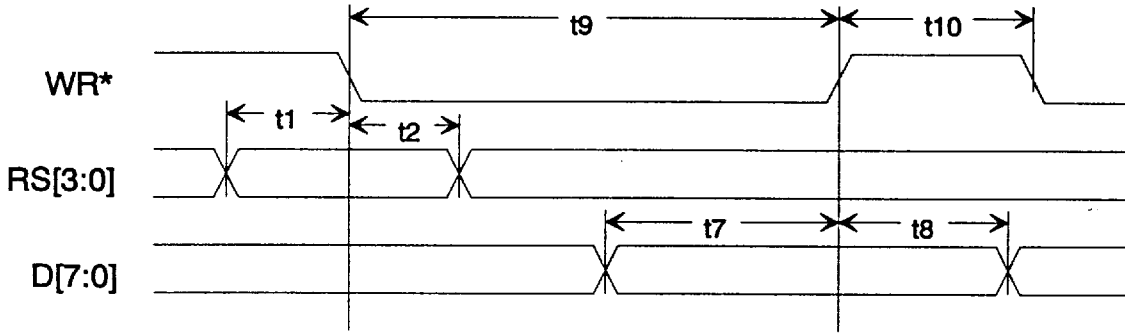


Figure 19: MPU Write Timing

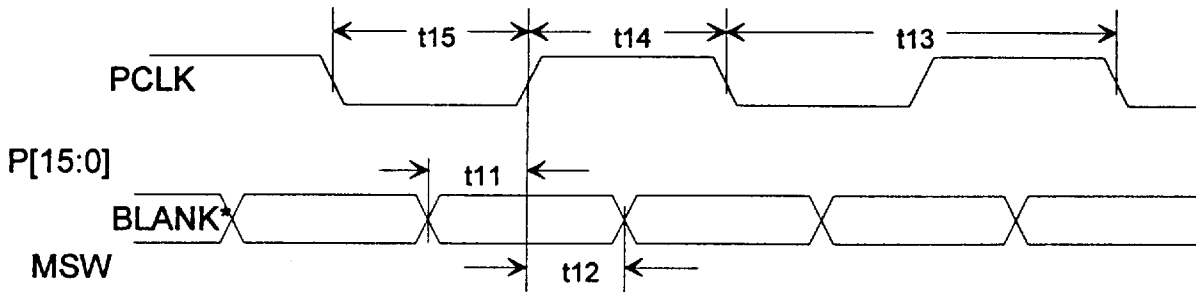


Figure 20: Pixel Data, BLANK* Control Signal, and Mode Switch Timing

Timing Diagrams (continued)

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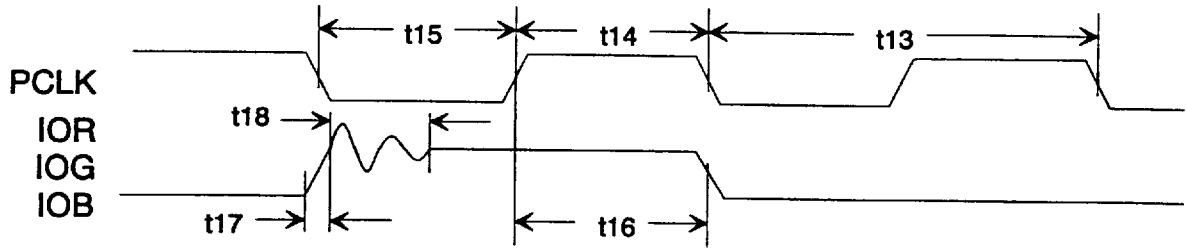


Figure 21: DAC Output Timing

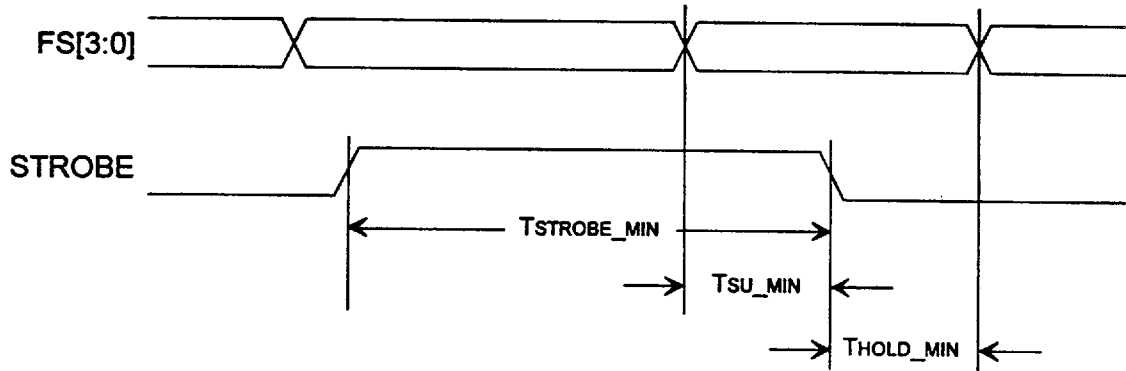


Figure 22: Strobe Timing

PC Board Layout Considerations

CH8398A is a high performance mixed signal IC containing precision analog and digital circuits. In order to achieve high performance, it is important to optimize the PC board layout (PCB) for the CH8398A. Care should be taken in laying out the power and ground planes to ensure good decoupling. In general, analog outputs should be short and wide to minimize inductive ringing, and analog signal traces crossover to digital signals should be minimized. When operating the device at high frequencies (> 50 MHz), the pixel data bus (P[15:0]) and the clock signals should have dedicated drivers. These signal traces should be kept short and placed beside each other the signal delays through the interconnects are matched, to minimize clock and data skew of the pixel bus.

Ground Planes

For four-layer PCBs with a uniform ground plane, CH8398A and its associated analog components (e.g., decoupling circuitry, current reference, and voltage reference) can be connected to the ground plane directly. The connections to the ground plane should be made with wide traces to minimize inductance. Connecting the analog and digital ground pins directly to the ground plane is highly recommended.

Supply Decoupling

For the digital power supply, bypass capacitors (0.1 μF) are recommended. Make leads as short as possible and place the capacitor as close as possible to the device. Connect the ground side of the capacitors directly to the ground plane.

For AVDD pin 42, a pi-filter configuration is recommended, with a 10 μF tantalum capacitor, in parallel with a 0.1 μF ceramic capacitor to GND, followed by a ferrite bead in series, then a 0.1 μF ceramic capacitor close to the AVDD pin.

For AVDD pin 3, a 5.1V zener diode with a 0.1 μF ceramic capacitor for supply conditioning that would result in optimal performance.

In general, short leads and direct connection to the power supply and ground planes are highly desirable. For details, please refer to **Figure 23** on page 47.

Digital Signal Interconnect

Place digital signals of the pixel bus, P[15:0] and PCLK, alongside each other to minimize data and clock skew. At high frequencies, these signals should have short traces, dedicated drivers, and series termination damping resistors to minimize signal reflections.

Analog Signal Interconnect

In general, analog signal traces should be as short as possible. Therefore, CH8398A should be located as close as possible to the VGA controllers and output connectors to minimize the amount of noise and transmission line reflection due to impedance mismatch between the PCB and the cable. Video outputs should overlay the analog ground plane to maximize supply rejection. To cut down the amount of transmission line reflection, connect a 75 Ω resistor with short leads between each video output and ground. Make the connection as close to the device as possible.

Some designs, such as VESA local bus, may have restrictions on component placement. For further discussion of this issue, please refer to "**Component Placement**" on page 50.

Clock Signals

In applications where either the video or memory clock frequencies are pushed toward the performance limit of the system, AC coupling circuitries should be used. This will allow for minor duty cycle adjustments for these high frequency signals. For additional information, please request a copy of AN-03, "**Application Notes on AC Coupling.**"

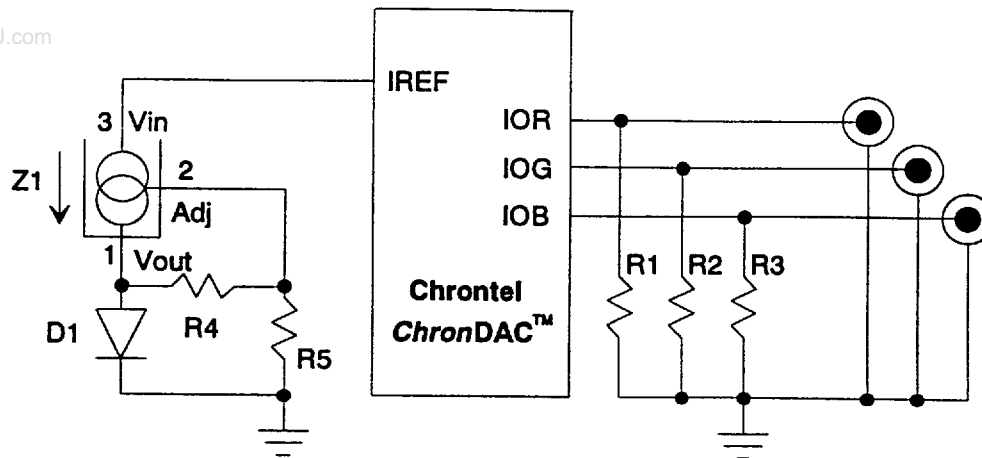


Figure 23: Typical Connection Using External Current Reference

Table 19 • List of Parts for Figure 23

| Symbol | Description |
|------------|--|
| D1 | 1N914 small signal diode |
| R1, R2, R3 | 75 Ω , metal film resistors |
| R4 | 18 Ω , 1/4W resistor |
| R5 | 180 Ω , 1/4W resistor |
| Z1 | LM334Z or equivalent current reference |

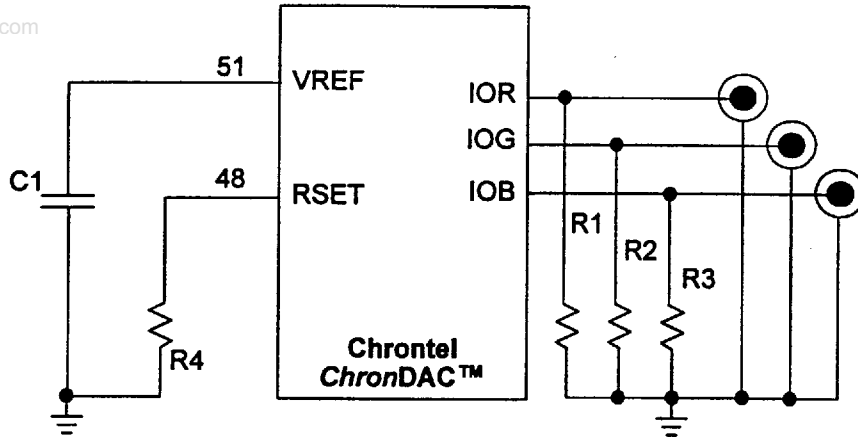


Figure 24: Typical Connection Using Internal Voltage Reference

Table 20 • List of Parts for Figure 24

| Symbol | Description |
|------------|------------------------------------|
| C1 | 0.1 μ F ceramic capacitor |
| R1, R2, R3 | 75 Ω , metal film resistors |
| R4 | 147 Ω , 1/4W resistor |

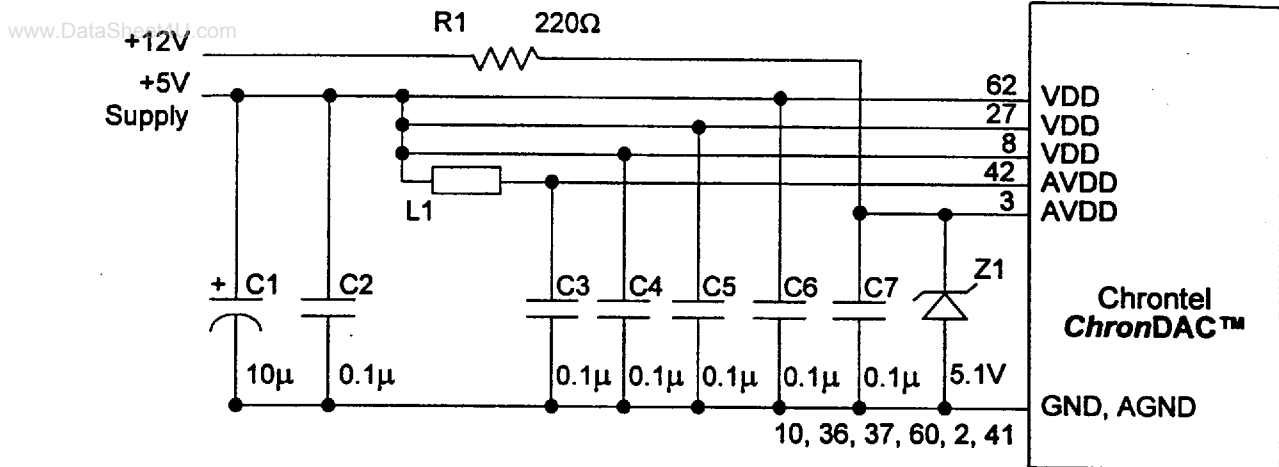


Figure 25: Recommended Supply Decoupling

Table 21 • List of Parts for Figure 25

| Symbol | Description |
|------------------------|--|
| C1 | 10 μF tantalum capacitor |
| C2, C3, C4, C5, C6, C7 | 0.1 μF ceramic capacitors |
| L1 | Ferrite bead |
| R1 | 220 Ω, 1/4W resistor |
| Z1 | 1N4733A 5.1V zener or equivalent current reference |

Component Placement

Figure 26 below is an example of typical placement of VGA components on a local bus VGA adapter. CH8398A should be placed as close as possible to the VGA controller, since there are high speed signals between these two devices. For most local bus implementation, the VGA controller will be placed in close proximity to the local bus connector. Due to the low impedance nature of the CH8398A RGB outputs, they can be located farther from the VGA monitor connector. Micro-strips or strip lines with characteristic impedance of 75 Ω should be used to route these outputs to the video connector.

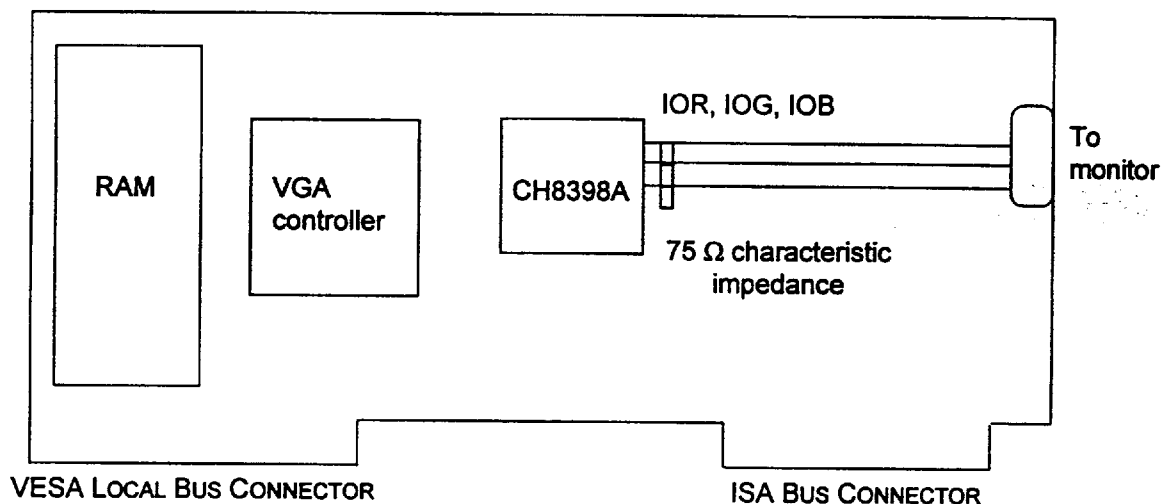


Figure 26: Recommended Placement of VGA Components for Local Bus VGA Adapter

| ORDERING INFORMATION | | | |
|----------------------|--------------|----------------|----------------|
| Part number | Package type | Number of pins | Voltage supply |
| CH8398A | PLCC | 68 | 5V |

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